

E77: VLSI Design Syllabus - Fall 2007

MWF 9:30-10:20, Hicks 211

Course Website: <http://www.swarthmore.edu/NatSci/tali/E77>

Instructor Information:

Prof. Tali Moreshet

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Office Hours:

TBA. Open door policy.

Course Description:

This course focuses on the design of complex digital systems, with an emphasis on hands-on chip design. We will cover both the bottom-up design approach, also known as full custom circuit design, and the top-down approach, also known as synthesis VLSI design.

Topics:

- Introduction to VLSI systems
- Review of digital systems
- CMOS logic and fabrication
- MOS transistor theory
- Layout design rules
- Circuit characterization and performance estimation
- Circuit simulation
- Combinational and sequential circuit design
- Static and dynamic CMOS gates
- Memory system design
- Design methodology and tools

Please check the course website for an updated course schedule, readings, labs and homework schedule.

Prerequisites: ENGR 15/CPSC 24 recommended.

Course Objectives:

- Design and implementation of CMOS digital circuits using CAD tools, including:
 - Gate-level design
 - Transistor-level design

- Layout
- Hierarchical design
- Verilog HDL design
- Logic synthesis
- Simulation and verification
- Circuit optimization with respect to area, performance and/or power consumption
- Avoiding design reliability problems

Required Textbook:

- Neil Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, third edition, Addison Wesley, 2005.

Labs, Exams & Grading:

The course has a midterm exam, bi-weekly homework assignments, 5 labs and a final project. Your homework should reflect your individual work. Labs will be done in groups of 2.

Grading will follow approximately the divisions shown below.

Homework:	10%
Labs:	35%
Final project:	20%
Midterm Exam:	25%
Class participation:	10%

Final Projects:

The final project consists of a full custom layout VLSI design project of your choice. The project can be completed in groups or individually. Students are expected to present their projects to the class.

Late Policy:

Homework and labs will be due at the beginning of class on the day specified. I will do my best to return your graded work in a timely manner, and I expect you to turn in your work on time. Substantial grade penalty will be given to work that is turned in late without advanced permission.