E24: VLSI Design
Syllabus - Fall 2011
T Th 8:30-9:45, Hicks 211

Course Website: http://www.swarthmore.edu/NatSci/tali/E24

Instructor Information:
Prof. Tali Moreshet
Office: Hicks 218
Phone (office): 328-8331
Email: tali@swarthmore.edu

Office Hours:
TBD. Open door policy.

Course Description:
This course focuses on the design of digital integrated systems, with an emphasis on hands-on chip design using CAD tools. We will focus on CMOS technology, and cover both full custom layout design and synthesis using Verilog. The course will also include an introduction to electronic design automation, which automates the design and test process of electronic systems. The following topics will be covered:

- Introduction to VLSI systems
- CMOS logic and fabrication
- MOS transistor theory
- Layout design rules
- Circuit characterization and performance estimation
- Circuit simulation
- Combinational and sequential circuit design
- Static and dynamic CMOS gates
- Memory system design
- Design methodology and tools

Please check the course website for an updated course schedule, readings, labs and homework schedule.

Prerequisites: ENGR 15.

Course Objectives:

- Design and implementation of CMOS digital circuits using CAD tools, including:
  - Gate and transistor-level design
  - Layout
  - Hierarchical design
- Verilog HDL design
- Logic synthesis
- Simulation and verification

- Circuit optimization with respect to area, performance and/or power consumption
- Avoiding design reliability problems

**Textbook:**


**Labs, Exams & Grading:**
The course has two midterm exams, bi-weekly homework assignments, 5 labs and a final project. Grading will follow approximately the divisions shown below.

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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</thead>
<tbody>
<tr>
<td>Homework</td>
<td>10%</td>
</tr>
<tr>
<td>Labs</td>
<td>30%</td>
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<tr>
<td>Final project</td>
<td>20%</td>
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<tr>
<td>Exams</td>
<td>2x15%</td>
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<tr>
<td>Class participation</td>
<td>10%</td>
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**Final Projects:**
The final project consists of a VLSI design project of your choice. The project can be completed in groups or individually. Students are expected to present their projects to the class.

**Late Policy:**
Homework and labs will be due at the beginning of class on the day specified. I will do my best to return your graded work in a timely manner, and I expect you to turn in your work on time. Substantial grade penalty will be given to work that is turned in late without advanced permission.

**Collaboration Policy:**

- It is legitimate to work together on homework, but not to copy. The homework you turn in should reflect your individual work.
- Labs will be done in groups of 2-3. You may discuss your lab report with other groups, but you may not copy anything from their reports.
- Any outside sources used for your lab reports (or homework, where appropriate), such as books and on-line resources, should be explicitly cited.