ENGR015 Laboratory
Fundamentals of Digital Systems
Fall 2014
Swarthmore Engineering
Mondays/Wednesdays
Lab: 5-8pm, Hicks 310

Course Description:
This is the laboratory of ENGR015. The course will introduce students to digital system theory and design techniques, including Boolean algebra, binary arithmetic, digital representation of data, gates, and truth tables. Digital systems include both combinational and sequential logic—consisting of flip-flops, finite state machines, memory, and timing issues. Students will gain experience with several levels of digital systems, from simple logic circuits to a hardware description language and interface programming in C.

Prerequisite: At least 1 credit in engineering or computer science or permission of the instructor.

Course Web Site: on Swarthmore Moodle

Reference Books: No textbook for the laboratory.

Instructor: Dr. Chen-Huan Chiang
Office: off campus, when on campus Hicks 309
Tel: 610-690-8331
Email: cchiang1@swarthmore.edu

Office Hours: 4:30-5pm and after lab on Mondays/Wednesdays, or by appointment.

Skype: In case of snow or any reason that in-class presence is not permitted;
or you need lab help outside lab hours
Skype account: chenhuan_temple

Accommodations Statement: If you believe that you need accommodations for a disability, please contact Leslie Hempling in the Office of Student Disability Services (Parrish 113) or email lhempl1@swarthmore.edu to arrange an appointment to discuss your needs. As appropriate, she will issue students with documented disabilities a formal Accommodations Letter. Since accommodations require early planning and are not retroactive, please contact her as soon as possible. For details about the accommodations process, visit the Student Disability Service Website at http://www.swarthmore.edu/academic-advising-support/welcome-to-student-disability-service.

You are also welcome to contact me privately to discuss your academic needs. However, all disability-related accommodations must be arranged through the Office of Student Disability Services.
Grading Policy:
No late assignments will be accepted!
No cheating and plagiarisms will be tolerated!

Policy on lab work:
- Two students (preferably) as a lab discussion group; however, you may also discuss with other groups if your group have exhausted your ideas to complete the work.
- Each group submits one lab report.
- Each student shall complete your own lab assignments (i.e., coding and design) while you are encouraged to work on the problem closely with your group member.
  - Exception: The term project is a group project.
- Lab grade is based on the combination of your own design coding, lab demo and group lab report.
  - For each assignment, you may get a different grade from your team member since I will interview each of you and examine your design during the lab demo.
- Any unfinished lab assignment and term project will result in an INC or F grade for this course.
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<th>Alternative Groups</th>
<th>Lab</th>
<th>Demo</th>
<th>Report due</th>
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<tr>
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<td>A</td>
<td>Tutorial#1: Digital Design Methodology &amp; Schematic design using Altera Quartus</td>
<td>Lab#1: Schematic design</td>
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**Tentative Schedule:**

1. **Week 1:**
   - **Date:** 9/1, 9/3
   - **Alternative Groups:** A
   - **Lab Demo Report due:**
   - **Tutorial#1:** Digital Design Methodology & Schematic design using Altera Quartus
   - **Lab#1:** Schematic design

2. **Week 2:**
   - **Date:** 9/8, 9/10
   - **Alternative Groups:** B
   - **Lab Demo Report due:**
   - **As above**

3. **Week 3:**
   - **Date:** 9/12
   - **Alternative Groups:** B
   - **Lab Demo Report due:**
   - **Last day to drop**

4. **Week 4:**
   - **Date:** 9/15, 9/17
   - **Alternative Groups:** A
   - **Lab Demo Report due:**
   - **Lab#1:** continued
   - **Tutorial#2:** Basic C programming using Code Composer Studio and MSP430
   - **Lab#2:** Finite State Machine (i.e. Controller) design in C

5. **Week 5:**
   - **Date:** 9/22, 9/24
   - **Alternative Groups:** B
   - **Lab Demo Report due:**
   - **As above**

6. **Week 6:**
   - **Date:** 10/6, 10/8
   - **Alternative Groups:** B
   - **Lab Demo Report due:**
   - **As above**

7. **Week 7:**
   - **Date:** 10/13, 10/15
   - **Alternative Groups:** B
   - **Lab Demo Report due:**
   - **Fall Break (no lab)**

8. **Week 8:**
   - **Date:** 10/20, 10/22
   - **Alternative Groups:** A
   - **Lab Demo Report due:**
   - **Lab#3:** continued
   - **Tutorial#4:** Finite State Machine design in Verilog
   - **Lab#4:** Finite State Machine (i.e. Controller) design in Verilog

9. **Week 9:**
   - **Date:** 10/27, 10/29
   - **Alternative Groups:** B
   - **Lab Demo Report due:**
   - **Lab Demo Report due**

10. **Week 10:**
    - **Date:** 11/3, 11/5
    - **Alternative Groups:** A
    - **Lab Demo Report due:**
    - **Lab#4:** continued
    - **Term project brainstorming**
    - **Tutorial#5:** Introduction to MSP430 Assembly Language
    - **Lab#5:** Design in MSP430 Assembly Language

11. **Week 11:**
    - **Date:** 11/10, 11/12
    - **Alternative Groups:** B
    - **Lab Demo Report due:**
    - **Lab Demo Report due**

12. **Week 12:**
    - **Date:** 11/17, 11/19
    - **Alternative Groups:** A
    - **Lab Demo Report due:**
    - **Lab#5:** continued
    - **Term project**
    - **Term project proposal**

13. **Week 13:**
    - **Date:** 11/24, 11/26
    - **Alternative Groups:** B
    - **Lab Demo Report due:**
    - **Lab Demo Report due**

14. **Week 14:**
    - **Date:** 12/1, 12/3
    - **Alternative Groups:** A/B
    - **Lab Demo Report due:**
    - **Term project presentation**
    - **Term project presentation**

15. **Week 15:**
    - **Date:** 12/8
    - **Alternative Groups:** B
    - **Lab Demo Report due:**
    - **No lab (make-up classes for Thanksgiving)**

16. **Week 16:**
    - **Date:** 12/10
    - **Alternative Groups:** B
    - **Lab Demo Report due:**
    - **Term project presentation: continued for B groups**

17. **Week 17:**
    - **Date:** 12/15, 12/17
    - **Alternative Groups:** B
    - **Lab Demo Report due:**
    - **No lab (final exam 12/12 to 12/20)**