These devices contain four independent 2-input NAND gates. The devices perform the Boolean function \( Y = \overline{A} \cdot \overline{B} \) or \( Y = \overline{A} + \overline{B} \) in positive logic.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
• Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

• Dependable Texas Instruments Quality and Reliability

Description

These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A H X L</td>
<td>Y</td>
</tr>
<tr>
<td>B H X L</td>
<td></td>
</tr>
<tr>
<td>A L L H</td>
<td></td>
</tr>
</tbody>
</table>

Logic Symbol†

†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

Logic Diagram (positive logic)

Y = A + B or Y = A + B
These devices contain six independent inverters.
Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C.

FUNCTION TABLE (each gate)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
</tr>
</tbody>
</table>

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE

(TOP VIEW)

SN54LS08, SN54S08 . . . FK PACKAGE

(TOP VIEW)

NC—No internal connection

logic diagram (positive logic)

\[ Y = A \cdot B \] or \[ Y = \overline{A} + B \]
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

**Description**

These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

**Function Table** (each gate)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

**Logic Symbol**

![Logic Symbol Diagram]

1 This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, or W packages.

**Logic Diagram**

![Logic Diagram]

**Positive Logic**

\[ Y = A + B \text{ or } Y = \frac{A}{A + B} \]
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

<table>
<thead>
<tr>
<th>TYPE</th>
<th>TYPICAL AVERAGE</th>
<th>TYPICAL</th>
<th>TYPICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PROPAGATION DELAY TIME</td>
<td>TOTAL POWER</td>
<td>DISSIPATION</td>
</tr>
<tr>
<td>'86</td>
<td>14 ns</td>
<td>150 mW</td>
<td></td>
</tr>
<tr>
<td>'LS86A</td>
<td>10 ns</td>
<td>30.5 mW</td>
<td></td>
</tr>
<tr>
<td>'S86</td>
<td>7 ns</td>
<td>250 mW</td>
<td></td>
</tr>
</tbody>
</table>

description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions Y = A ⊕ B = ĀB + AĀ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN5486, 54LS86A, and the SN54S86 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7486, SN74LS86A, and the SN74S86 are characterized for operation from 0°C to 70°C.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

These are five equivalent Exclusive-OR symbols valid for an '86 or 'LS86A gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT

The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.
• Counts 8-4-2-1 BCD or Binary
• Single Down/Up Count Control Line
• Count Enable Control Input
• Ripple Clock Output for Cascading
• Asynchronously Presetable with Load Control
• Parallel Outputs
• Cascadable for n-Bit Applications

<table>
<thead>
<tr>
<th>TYPE</th>
<th>AVERAGE PROPAGATION DELAY</th>
<th>MAXIMUM CLOCK FREQUENCY</th>
<th>TYPICAL POWER DISSIPATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>'190, '191</td>
<td>20 ns</td>
<td>25MHz</td>
<td>325mW</td>
</tr>
<tr>
<td>'LS190, 'LS191</td>
<td>20 ns</td>
<td>25MHz</td>
<td>100mW</td>
</tr>
</tbody>
</table>

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.