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Safety Information

Regulatory Compliance

The CY8CKIT-042 PSoC® 4 Pioneer Kit is intended for use as a development platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure. Due to this reason, the board may cause interference to other electrical or electronic devices in close proximity. In a domestic environment, this product may cause radio interference. In such cases, the user may be required to take adequate preventive measures. Also, this board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

The CY8CKIT-042 as shipped from the factory has been verified to meet with requirements of CE as a Class A product.

The CY8CKIT-042 contains electrostatic discharge (ESD) sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY8CKIT-042 boards in the protective shipping package.

End-of-Life/Product Recycling

This kit has an end-of-life cycle five years from the date of manufacturing mentioned on the back of the box. Contact your nearest recycler for discarding the kit.
General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that the user perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Boards

CY8CKIT-042 boards are sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static free surface. Use a conductive foam pad if available. Do not slide board over any surface.
1. Introduction

Thank you for your interest in the PSoC® 4 Pioneer Kit. The kit is designed as an easy-to-use and inexpensive development kit, showcasing the unique flexibility of the PSoC 4 architecture. Designed for flexibility, this kit offers footprint-compatibility with several third-party Arduino™ shields. This kit has a provision to populate an extra header to support Digilent® Pmod™ peripheral modules. In addition, the board features a CapSense® slider, an RGB LED, a push button switch, an integrated USB programmer, a program and debug header, and USB-UART/I2C bridges. This kit supports either 5 V or 3.3 V as power supply voltages.

The PSoC 4 Pioneer Kit is based on the PSoC 4200 device family, delivering a programmable platform for a wide range of embedded applications. The PSoC 4 is a scalable and reconfigurable platform architecture for a family of mixed-signal programmable embedded system controllers with an ARM® Cortex™-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing.

1.1 Kit Contents

The PSoC 4 Pioneer kit contains:

- PSoC 4 Pioneer board
- Quick start guide
- USB standard A to mini-B cable
- Jumper wires
Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help: www.cypress.com/go/support.
1.2 PSoC Creator™

PSoC Creator is a state-of-the-art, easy-to-use integrated design environment (IDE). It introduces revolutionary hardware and software co-design, powered by a library of pre-verified and pre-characterized PSoC Components™.

With PSoC Creator, you can:
- Drag and drop PSoC components to build a schematic of your custom design
- Automatically place and route components and configure GPIOs
- Develop and debug firmware using the included component APIs

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler chains and production programmers for PSoC devices.

For more information, visit www.cypress.com/Creator.

1.3 Getting Started

This guide helps you to get acquainted with the PSoC 4 Pioneer Kit. The Software Installation chapter on page 11 describes the installation of the kit software. The Kit Operation chapter on page 17 explains how to program the PSoC 4 with a programmer and debugger – either the onboard PSoC 5LP or the external MiniProg3 (CY8CKIT-002). The Hardware chapter on page 27 details the hardware operation. The Code Examples chapter on page 43 describes the code examples. The Advanced Topics chapter on page 63 deals with topics such as building projects for PSoC 5LP, USB-UART functionality, and USB-I2C functionality of PSoC 5LP. The Appendix on page 101 provides the schematics, pin assignment, use of zero-ohm resistors, troubleshooting, and the bill of materials (BOM).

1.4 Additional Learning Resources

Visit www.cypress.com/PSoC4 for additional learning resources in the form of datasheets, technical reference manual, and application notes.
- Beginner resources – PSoC Creator Training: www.cypress.com/go/creatorstart/creatortraining
- Engineers looking for more – Visit www.cypress.com/appnotes to view a growing list of application notes for PSoC 3, PSoC 4, and PSoC 5LP.
- Learning from peers – Cypress Developer Community Forums: www.cypress.com/forums

1.5 Technical Support

For assistance, go to our support web page, www.cypress.com/support, or contact our customer support at +1 (800) 541-4736 Ext. 8 (in the USA) or +1 (408) 943-2600 Ext. 8 (International).
1.6 Document Revision History

Table 1-1. Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Issue Date</th>
<th>Origin of Change</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>04/23/2013</td>
<td>ANCY</td>
<td>Initial version of kit guide.</td>
</tr>
<tr>
<td>*A</td>
<td>04/25/2013</td>
<td>ANCY</td>
<td>Minor changes across the guide.</td>
</tr>
<tr>
<td>*B</td>
<td>05/23/2013</td>
<td>RKAD</td>
<td>Updated Figure 1-1 and minor changes across the guide. Added PSoC 5LP Factory Program Restore Instructions on page 93.</td>
</tr>
<tr>
<td>*C</td>
<td>08/23/2013</td>
<td>SASH</td>
<td>Updated Figure 5-2 and Figure 5-3. Minor changes across the guide.</td>
</tr>
<tr>
<td>*D</td>
<td>11/26/2013</td>
<td>SASH</td>
<td>Updated PSoC Creator training web link. Updated PSoC Creator images; added figure captions. Modified the CapSense code example.</td>
</tr>
</tbody>
</table>

1.7 Documentation Conventions

Table 1-2. Document Conventions for Guides

<table>
<thead>
<tr>
<th>Convention</th>
<th>Usage</th>
</tr>
</thead>
</table>
|Courier New        | Displays file locations, user entered text, and source code:  
|                   | C:\ ...cd\icc\                                                        |
|Italics            | Displays file names and reference documentation:  
|                   | Read about the sourcefile.hex file in the PSoC Designer User Guide. |
|[Bracketed, Bold]   | Displays keyboard commands in procedures:  
|                   | [Enter] or [Ctrl] [C]                                                 |
|File > Open        | Represents menu paths:  
|                   | File > Open > New Project                                             |
|Bold               | Displays commands, menu paths, and icon names in procedures:  
|                   | Click the File icon and then click Open.                            |
|Times New Roman    | Displays an equation:  
|                   | 2 + 2 = 4                                                           |
|Text in gray boxes | Describes cautions or unique functionality of the product.            |
2. Software Installation

2.1 Install Kit Software

Follow these steps to install the PSoC 4 Pioneer Kit software:
2. Select the folder to install the CY8CKIT-042 related files. Choose the directory and click **Next**.

Figure 2-1. Installation Folder
3. Select the installation type and click **Next**.

**Figure 2-2. Installation Type Options**

- **Product Installation Overview**

After the installation is complete, the kit contents are available at the following location:

<Install_Directory>:\CY8CKIT-042 PSoC 4 Pioneer Kit\<version>

**Note** For Windows 7 users, the installed files and the folder are read-only. To change the property, right-click the folder and select **Properties > Attributes**, disable the **Read-only** radio button. Click **Apply** and **OK** to close the window.

### 2.2 Install Hardware

There is no additional hardware installation required for this kit.

### 2.3 Install Software

When installing the PSoC 4 Pioneer Kit, the installer checks if the required software is installed in the system. If the required applications are not installed, then the installer prompts you to download and install them.

The following software is required:

- **PSoC Creator 3.0 or later:** Download the latest software from [www.cypress.com/go/Creator](http://www.cypress.com/go/Creator).
- **PSoC Programmer 3.19.1 or later:** Download the latest software from [www.cypress.com/go/Programmer](http://www.cypress.com/go/Programmer).
- **Code examples:** After the kit installation is complete, the code examples are available in the kit firmware folder. Download the CD ISO image or the setup files to install the kit from [www.cypress.com/go/CY8CKIT-042](http://www.cypress.com/go/CY8CKIT-042).
2.4 Uninstall Software

The software can be uninstalled using one of the following methods:

■ Go to Start > All Programs > Cypress > Cypress Update Manager > Cypress Update Manager; select the Uninstall button.
■ Go to Start > Control Panel > Programs and Features; select the Uninstall/Change button.

2.5 Develop Code Fast and Easy with Code Examples

PSoC Creator provides several example projects that make code development fast and easy. To access these projects, click Find Example Project... under the Example and Kits section in the Start Page of PSoC Creator or navigate to the Creator tool bar and select File > Example Project.

Figure 2-3. Find Example Project

The Find Example Project section has various filters that help to locate the most relevant project.
PSoC Creator also provides several starter designs for each device family. These designs highlight features that are unique to each PSoC family. They provide users with a starting place instead of creating a new empty design. These starter projects come loaded with various pre-selected components. To use a starter design, navigate to File > New > Project and select the design required.
In addition to the example projects and starter designs that are available within PSoC Creator, Cypress continuously strives to provide the best support. Click here to view a growing list of application notes for PSoC 3, PSoC 4, and PSoC 5LP.
2.6 Open an Example Project in PSoC Creator

1. Launch PSoC Creator from the Start menu.

Figure 2-5. PSoC Creator Start Page

2. Open the example project from the Start Page by clicking <Project.cywrk> present below the Examples and Kits > Kits > CY8CKIT-042.

Figure 2-6. Open Example Project
3. The example project opens and displays the project files in the Workspace Explorer. Subsequent sections of this user guide describe how to build, program, and understand the example projects supported in this kit.

Figure 2-7. Workspace Explorer
3. Kit Operation

The PSoC 4 Pioneer Kit can be used to develop applications using the PSoC 4 family of devices and the Arduino shields and Digilent Pmod daughter cards. Figure 3-1 is an image of the PSoC 4 Pioneer board with a markup of the onboard components.

Figure 3-1. PSoC 4 Pioneer Board
3.1 **Pioneer Kit USB Connection**

The PSoC 4 Pioneer Kit connects to the PC over a USB interface. The kit enumerates as a composite device and three separate devices appear under the Device Manager window in the Windows operating system.

<table>
<thead>
<tr>
<th>Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB Input Device</td>
<td>USB-I2C bridge</td>
</tr>
<tr>
<td>KitProg</td>
<td>Programmer and debugger</td>
</tr>
<tr>
<td>KitProg USB-UART</td>
<td>USB-UART bridge will appear as a COM# port</td>
</tr>
</tbody>
</table>

Figure 3-2. KitProg Driver Installation

Figure 3-3. KitProg Driver Installation
3.2 Programming and Debugging PSoC 4

The kit allows programming and debugging of the PSoC 4 device in two modes:
- Using the onboard PSoC 5LP programmer and debugger
- Using a CY8CKIT-002 MiniProg3 programmer and debugger

3.2.1 Using the Onboard PSoC 5LP Programmer and Debugger

The default programming interface for the kit is a USB-based, onboard programming interface. Before trying to program the device, PSoC Creator and PSoC Programmer must be installed. See Install Software on page 12 for information on installing the kit software.

1. To program the device, plug the USB cable into the programming USB connector J10, as shown in Figure 3-4. The kit will enumerate as a composite device. See Pioneer Kit USB Connection on page 18 for details.

Figure 3-4. Connect USB Cable to J10

2. The onboard PSoC 5LP uses serial wire debug (SWD) to program the PSoC 4 device. See Figure 3-5 for this implementation.

Figure 3-5. SWD Programming PSoC 4 Using PSoC 5LP
Kit Operation

3. The Pioneer Kit’s onboard programmer will enumerate on the PC and in the software tools as **KitProg**. Load an example project in PSoC Creator (such as the project described in Install Software on page 12) and initiate the build by clicking Build > Build Project or [Shift]+[F6].

Figure 3-6. Build Project in PSoC Creator

![Build Project in PSoC Creator](image)

4. After the project is built without errors and warnings, select Debug > Program or [Ctrl]+[F5] to program the device.

Figure 3-7. Program Device from PSoC Creator

![Program Device from PSoC Creator](image)

The onboard programmer supports only the RESET programming mode. When using the onboard programmer, the board can either be powered by the USB (VBUS) or by an external source such as an Arduino shield. If the board is already powered from another source, plugging in the USB programmer does not damage the board.
3.2.2 Using CY8CKIT-002 MiniProg3 Programmer and Debugger

The PSoC 4 on the Pioneer Kit can also be programmed using a MiniProg3 (CY8CKIT-002). To use MiniProg3 for programming, use the J6 connector on the board, as shown in Figure 3-8. With MiniProg3, programming is similar to the onboard programmer; however, the setup enumerates as a MiniProg3. Only the RESET programming mode is available.

The board can also be powered from the MiniProg3. To do this, select Tool > Options. In the Options window, expand Program and Debug > Port Configuration; click MiniProg3 and select the settings shown in Figure 3-9. Click Debug > Program to program and power the board.

Note The CY8CKIT-002 MiniProg3 is not part of the PSoC 4 Pioneer Kit contents. It can be purchased from the Cypress Online Store.

Figure 3-8. PSoC 4 Programming/Debug Using MiniProg3
3.3 USB-UART Bridge

The onboard PSoC 5LP can also act as a USB-UART bridge to transfer and receive data from the PSoC 4 device to the PC via the COM terminal software. When the USB mini-B cable is connected to J10 of the PSoC 4 Pioneer Kit, a device named KitProg USBUART is available under Ports (COM & LPT) in the device manager. For more details about the USB-UART functionality, see Using PSoC 5LP as USB-UART Bridge on page 63.

To use the USB-UART functionality in the COM terminal software, select the corresponding COM port as the communication port for transferring data to and from the COM terminal software.

The UART lines from PSoC 5LP are brought to the P12[6] (J8_9) and P12[7] (J8_10) pins of header J8. This interface can be used to send or receive data from any PSoC 4 design that has a UART by connecting the pins on header J8 to the RX and TX pins assigned in PSoC 4. The UART can be used as an additional interface to debug designs. This bridge can also be used to interface with other external UART-based devices. Figure 3-10 shows the connection between the RX and TX lines of the PSoC 5LP and PSoC 4. In this example, the PSoC 4 UART has been routed to the J3 header; the user must connect the wires between the PSoC 5LP RX and TX lines available on header J8.
Table 3-2 lists the specifications supported by the USB-UART bridge.

Table 3-2. Specifications Supported by USB-UART Bridge

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Supported Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud Rate</td>
<td>1200, 2400, 4800, 9600, 19200, 38400, 57600, and 115200</td>
</tr>
<tr>
<td>Data Bits</td>
<td>8</td>
</tr>
<tr>
<td>Parity</td>
<td>None</td>
</tr>
<tr>
<td>Stop Bits</td>
<td>1</td>
</tr>
<tr>
<td>Flow Control</td>
<td>None</td>
</tr>
<tr>
<td>File transfer protocols supported</td>
<td>Xmodem, 1K Xmodem, Ymodem, Kermit, and Zmodem (only speeds greater than 2400 baud).</td>
</tr>
</tbody>
</table>
3.4 USB-I2C Bridge

The PSoC 5LP also functions as a USB-I2C bridge. The PSoC 4 communicates with the PSoC 5LP using an I2C interface and the PSoC 5LP transfers the data over the USB to the USB-I2C software utility on the PC, called the Bridge Control Panel (BCP).

The BCP is available as part of the PSoC Programmer installation. This software can be used to send and receive USB-I2C data from the PSoC 5LP. When the USB mini-B cable is connected to header J10 on the Pioneer Kit, the KitProg USB-I2C is available under Connected I2C/SPI/RX8 Ports in the BCP.

Figure 3-11. Bridge Control Panel

To use the USB-I2C functionality, select the KitProg USB-I2C in the BCP. On successful connection, the Connected and Powered tabs turn green.
Kit Operation

3.5 Updating the Onboard Programmer Firmware

The firmware of the onboard programmer and debugger, PSoC 5LP, can be updated from PSoC Programmer. When a new firmware is available or when the KitProg firmware is corrupt (see Error in Firmware/Status Indication in Status LED on page 107), PSoC Programmer displays a warning indicating that new firmware is available.

Open PSoC Programmer from Start > All Programs > Cypress > PSoC Programmer<version>. When PSoC Programmer opens, a WARNING! window pops up saying that the programmer is currently out of date.

Figure 3-12. KitProg USB-I2C Connected in Bridge Control Panel

USB-I2C is implemented using the USB and I2C components of PSoC 5LP. The SCL (P12_0) and SDA (P12_1) lines from the PSoC 5LP are connected to SCL (P3_0) and SDA (P3_1) lines of the PSoC 4 I2C. The USB-I2C bridge currently supports I2C speed of 50 kHz, 100 kHz, 400 kHz, and 1 MHz.

Refer to Using PSoC 5LP as USB-I2C Bridge on page 76 for building a project, which uses USB-I2C Bridge functionality.

Figure 3-13. Firmware Update Warning
Click **OK** to close the window. On closing the warning window, the **Action and Results** window displays "Please navigate to the Utilities tab and click the Upgrade Firmware button".

Figure 3-14. Upgrade Firmware Message in PSoC Programmer

![Figure 3-14. Upgrade Firmware Message in PSoC Programmer](image)

Click the **Utilities** tab and click the **Upgrade Firmware** button. On successful upgrade, the **Action and Results** window displays the firmware update message with the KitProg version.

Figure 3-15. Firmware Updated in PSoC Programmer

![Figure 3-15. Firmware Updated in PSoC Programmer](image)
4. Hardware

4.1 Board Details

The PSoC 4 Pioneer Kit consists of the following blocks:

- PSoC 4
- PSoC 5LP
- Power supply system
- Programming interfaces (J6, J7 - unpopulated, J10)
- Arduino compatible headers (J1, J2, J3, J4, and J12 - unpopulated)
- Digilent Pmod compatible header (J5 - unpopulated)
- PSoC 5LP GPIO header (J8)
- CapSense slider
- Pioneer board LEDs
- Push buttons (Reset and User buttons)

Figure 4-1. PSoC 4 Pioneer Kit Details
Figure 4-2. PSoC 4 Pioneer Kit Pin Mapping
4.2 Theory of Operation

This section provides the block-level description of the PSoC 4 Pioneer Kit.

Figure 4-3. Block Diagram

The PSoC 4 is a new generation of programmable system-on-chip devices from Cypress for embedded applications. It combines programmable analog, programmable digital logic, programmable I/O, and a high-performance ARM Cortex-M0 subsystem. With the PSoC 4, you can create the combination of peripherals required to meet the application specifications.

The PSoC 4 Pioneer Kit features an onboard PSoC 5LP, which communicates through the USB to program and debug the PSoC 4 using serial wire debug (SWD). The PSoC 5LP also functions as a USB-I2C bridge and USB-UART bridge.

The Pioneer Kit has an RGB LED, a status LED, and a power LED. The RGB LED is connected to the PSoC 4 and the status LED is connected to the PSoC 5LP. For more information on the status LED, see section A.5 Error in Firmware/Status Indication in Status LED on page 107. This kit also includes a reset button that connects to the PSoC 4 XRES, a user button, and a five-segment CapSense slider, which can be used to develop touch-based applications. The PSoC 4 pins are brought out onto headers J1 to J4 on the kit to support Arduino shields. The PSoC 5LP pins are brought out onto header J8 to enable using the onboard PSoC 5LP to develop custom applications.

The PSoC 4 Pioneer Kit can be powered from the USB Mini B, the Arduino compatible header, or an external power supply. The input voltage is regulated by a low drop-out (LDO) regulator to 3.3 V. You can select between VBUS (5 V) and 3.3 V by suitably plugging the jumper onto the voltage selection header VDD.
4.3 Functional Description

4.3.1 PSoC 4

This kit uses the PSoC 4200 family device. PSoC 4200 devices are a combination of a microcontroller with programmable logic, high-performance analog-to-digital conversion, two opamps with comparator mode, and commonly used fixed-function peripherals. For more information, refer to the PSoC 4 web page and the PSoC 4200 family datasheet.

Features

- 32-bit MCU subsystem
  - 48 MHz ARM Cortex-M0 CPU with single cycle multiply
  - Up to 32 KB of flash with read accelerator
  - Up to 4 KB of SRAM
- Programmable analog
  - Two opamps with reconfigurable high-drive external and high-bandwidth internal drive, comparator modes, and ADC input buffering capability
  - 12-bit 1-Msps SAR ADC with differential and single-ended modes; channel sequencer with signal averaging
  - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
  - Two low-power comparators that operate in deep sleep
- Programmable digital
  - Four programmable logic blocks called universal digital blocks (UDBs), each with eight Macro-cells and data path
  - Cypress-provided peripheral component library, user-defined state machines, and Verilog input
- Low power 1.71 to 5.5 V operation
  - 20-nA Stop mode with GPIO pin wakeup
  - Hibernate and Deep-Sleep modes allow wakeup-time versus power trade-offs
- Capacitive sensing
  - Cypress Capacitive Sigma-Delta (CSD) provides best-in-class SNR (greater than 5:1) and water tolerance
  - Cypress-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense™)
- Segment LCD drive
  - LCD drive supported on all pins (common or segment)
  - Operates in Deep-Sleep mode with 4 bits per pin memory
- Serial communication
  - Two independent run-time reconfigurable serial communication blocks (SCBs) with re-configurable I2C, SPI, or UART functionality
- Timing and pulse-width modulation
  - Four 16-bit Timer/Counter Pulse-Width Modulator (TCPWM) blocks
  - Center-aligned, Edge, and Pseudo-random modes
  - Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications
- Up to 36 programmable GPIOs
  - 44-pin TQFP, 40-pin QFN, and 28-pin SSOP packages
  - Any GPIO pin can be Capsense, LCD, analog, or digital
  - Drive modes, strengths, and slew rates are programmable
- PSoC Creator design environment
  - Integrated development environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
Applications Programming Interface (API) component for all fixed-function and programmable peripherals

Industry-standard tool compatibility

After schematic entry, development can be done with ARM-based industry-standard development tools

For more information see the CY8C42 family datasheet.

4.3.2 PSoC 5LP

An onboard PSoC 5LP is used to program and debug PSoC 4. The PSoC 5LP connects to the USB port of the PC through a USB Mini B connector and to the SWD interface of the PSoC 4 device.

PSoC 5LP is a true system-level solution providing MCU, memory, analog, and digital peripheral functions in a single chip. The CY8C58LPxx family offers a modern method of signal acquisition, signal processing, and control with high accuracy, high bandwidth, and high flexibility. Analog capability spans the range from thermocouples (near DC voltages) to ultrasonic signals. For more information, refer to the PSoC 5LP web page.

Features

- 32-bit ARM Cortex-M3 CPU core
  - DC to 67-MHz operation
  - Flash program memory, up to 256 KB, 100,000 write cycles, 20-year retention, and multiple security features
  - Up to 32-KB flash error correcting code (ECC) or configuration storage
  - Up to 64 KB SRAM
  - 2-KB electrically erasable programmable read-only memory (EEPROM) memory, 1 M cycles, and 20 years retention
  - 24-channel direct memory access (DMA) with multilayer AHB bus access
    a. Programmable chained descriptors and priorities
    b. High bandwidth 32-bit transfer support

- Low voltage, ultra low power
  - Wide operating voltage range: 0.5 V to 5.5 V
  - High-efficiency boost regulator from 0.5 V input to 1.8 V to 5.0 V output
  - 3.1 mA at 6 MHz
  - Low power modes including:
    a. 2-µA sleep mode with real time clock (RTC) and low-voltage detect (LVD) interrupt
    b. 300-nA hibernate mode with RAM retention

- Versatile I/O system
  - 28 to 72 I/Os (62 GPIOs, 8 SIOs, 2 USBIOs)
  - Any GPIO to any digital or analog peripheral routability
  - LCD direct drive from any GPIO, up to 46×16 segments
  - CapSense support from any GPIO[3]
  - 1.2 V to 5.5 V I/O interface voltages, up to 4 domains
  - Maskable, independent IRQ on any pin or port
  - Schmitt-trigger transistor-transistor logic (TTL) inputs
  - All GPIOs configurable as open drain high/low, pull-up/pull-down, High-Z, or strong output
  - Configurable GPIO pin state at power-on reset (POR)
  - 25 mA sink on SIO

- Digital peripherals
  - 20 to 24 programmable logic device (PLD) based universal digital blocks (UDBs)
  - Full CAN 2.0b 16 RX, 8 TX buffers
  - Full-Speed (FS) USB 2.0 12 Mbps using internal oscillator
Hardware

- Four 16-bit configurable timers, counters, and PWM blocks
- 67-MHz, 24-bit fixed point digital filter block (DFB) to implement finite impulse response (FIR) and infinite impulse response (IIR) filters
- Library of standard peripherals
  - a. 8-, 16-, 24-, and 32-bit timers, counters, and PWMs
  - b. Serial peripheral interface (SPI), universal asynchronous transmitter receiver (UART), and I2C
  - c. Many others available in catalog
- Library of advanced peripherals
  - a. Cyclic redundancy check (CRC)
  - b. Pseudo random sequence (PRS) generator
  - c. Local interconnect network (LIN) bus 2.0
  - d. Quadrature decoder
- Analog peripherals (1.71 V \( \leq \) VDDA \( \leq \) 5.5 V)
  - 1.024 V ±0.1% internal voltage reference across –40 °C to +85 °C
- Configurable delta-sigma ADC with 8- to 20-bit resolution
  - Sample rates up to 192 kps
  - Programmable gain stage: ×0.25 to ×16
  - 12-bit mode, 192 kps, 66-dB signal to noise and distortion ratio (SINAD), ±1-bit INL/DNL
  - 16-bit mode, 48 kps, 84-dB SINAD, ±2-bit INL, ±1-bit DNL
  - Up to two SAR ADCs, each 12-bit at 1 Mspss
  - Four 8-bit 8 Mspss current IDACs or 1-Mspss voltage VDACs
  - Four comparators with 95-ns response time
  - Four uncommitted opamps with 25-mA drive capability
  - Four configurable multifunction analog blocks. Example configurations are programmable gain amplifier (PGA), transimpedance amplifier (TIA), mixer, and sample and hold
  - CapSense support
- Programming, debug, and trace
  - JTAG (4 wire), SWD (2 wire), single wire viewer (SWV), and TRACEPORT interfaces
  - Cortex-M3 flash patch and breakpoint (FPB) block
  - Cortex-M3 Embedded Trace Macrocell™ (ETM™) generates an instruction trace stream
  - Cortex-M3 data watchpoint and trace (DWT) generates data trace information
  - Cortex-M3 Instrumentation Trace Macrocell (ITM) can be used for printf-style debugging
  - DWT, ETM, and ITM blocks communicate with off-chip debug and trace systems via the SWV or TRACEPORT
  - Bootloader programming supportable through I2C, SPI, UART, USB, and other interfaces
- Precision, programmable clocking
  - 3- to 62-MHz internal oscillator over full temperature and voltage range
  - 4- to 25-MHz crystal oscillator for crystal PPM accuracy
  - Internal PLL clock generation up to 67 MHz
  - 32.768-kHz watch crystal oscillator
  - Low-power internal oscillator at 1, 33, and 100 kHz

For more, see the CY8C58LPxx family datasheet.
4.3.3 Power Supply System

The power supply system on this board is versatile, allowing the input supply to come from the following sources:

- 5-V power from onboard USB programming header J10
- 5-V to 12-V power from Arduino shield using J1_01 header
- VTARG - power from the onboard SWD programming using J6 or J7
- VIN - J11

The PSoC 4 and PSoC 5LP are powered with either a 3.3 V or 5 V source. The selection between 3.3 V and 5 V is made through the J9 jumper. The board can supply 3.3 V and 5 V to the I/O headers and receive 3.3 V from the I/O headers. The board can also be powered with an external power supply through the VIN (J11) header; the allowed voltage range for the VIN is 5 V to 12 V. The LDO regulator regulates the VIN down to 3.3 V. Figure 4-4 shows the power supply block diagram and protection circuitry.

Note: The 5-V domain is directly powered by the USB (VBUS). For this reason, this domain is unregulated.

Figure 4-4. Power Supply Block Diagram with Protection Circuits
4.3.3.1 Protection Circuit

The power supply rail has reverse-voltage, over-voltage, short circuits, and excess current protection features, as seen in Figure 4-4.

- The Schottky diode (D1) ensures power cannot be supplied to the 5-V domain of the board from the I/O header.
- The series protection diode (D2) ensures VIN (power supply from the I/O header) does not back power the USB.
- The Schottky diode (D3) ensures 3.3 V from I/O header does not back power the LDO.
- The series protection diode (D4) ensures that the reverse-voltage cannot be supplied from the VIN to the regulator input.
- A PTC resettable fuse is connected to protect the computer's USB ports from shorts and overcurrent.
- The MOSFET-based protection circuit provides over-voltage and reverse-voltage protection to the 3.3-V rail. The PMOS Q1 protects the board components from a reverse-voltage condition. The PMOS Q2 protects the PSoC from an over-voltage condition. The PMOS Q2 will turn off when a voltage greater than 4.2 V is applied, protecting the PSoC 4.
- The output voltage of the LDO is adjusted such that it takes into account the voltage drop across the Schottky diode and provides 3.3 V.

4.3.3.2 Procedure to Measure PSoC 4 Current Consumption

The following three methods are supported for measuring current consumption of the PSoC 4 device.

- When the board is powered through the USB port (J10), remove jumper J13 and connect an ammeter, as shown in Figure 4-5.

Figure 4-5. PSoC 4 Current Measurement when Powered from USB Port

- When using a separate power supply for the PSoC 4 with USB powering (regulator output on the USB supply must be within 0.5 V of the separate power supply).
  - Remove jumper J13. Connect the positive terminal of voltage supply to the positive terminal of the ammeter and the negative terminal of the ammeter to the lower pin of J13. Figure 4-6 shows the required connections.
When the PSoC 4 is powered separately and the PSoC 5LP is not powered, make these changes to avoid leakage while measuring current:

- Remove the zero-ohm resistors R24 and R25. Removing these resistors will affect the USB-I2C functionality.
- Remove R11, R15, and R16, which are meant for programming the PSoC 4. Removing these resistors disables the PSoC 5LP capability for programming.
- Connect an ammeter between pins 1 and 2 of header J13 to measure current.

4.3.4 Programming Interface

The kit allows programming and debugging of the PSoC 4 in two modes:

- Using the Onboard PSoC 5LP Programmer and Debugger
- Using CY8CKIT-002 MiniProg3 Programmer and Debugger
4.3.5 Arduino Compatible Headers (J1, J2, J3, J4, and J12 - unpopulated)

This kit has five Arduino compatible headers; J1, J2, J3, J4 and J12. You can develop applications based on the Arduino shield's hardware.

Figure 4-8. Arduino Header

The J1 header contains I/O pins for reset, internal reference voltage (VREF), and power supply line. The J2 header is an analog port. It contains I/O pins for SAR ADC, comparator, and opamp. The J3 header is primarily a digital port. It contains I/O pins for PWM, I2C, SPI, and analog reference. The J4 header is also a digital port. It contains I/O pins for UART and PWM. The J12 header is an Arduino ICSP compatible header for the SPI interface. This header is not populated. Refer to the “No Load Components” section of A.6 Bill of Materials (BOM) on page 108 for the header part number.
4.3.5.1 Additional Functionality of Header J2

The J2 header is a 9×2 header that supports Arduino shields. The port 0, port 1, and port 2 pins of PSoC 4 are brought to this header. The port 1 pins additionally connect to the onboard CapSense slider through 560-Ω resistors. When the CapSense feature is not used, remove these resistors to ensure a better performance with these pins.
4.3.5.2 Functionality of Unpopulated Header J12

The J12 header is a 2×3 header that supports Arduino shields. This header is used on a small subset of shields and is unpopulated on the PSoC 4 Pioneer Kit. Note that the J12 header only functions in 5.0 V mode. To ensure proper shield functionality, ensure the power jumper is connected in 5.0 V mode.

4.3.6 Digilent Pmod Compatible Header (J5 - unpopulated)

This port supports Digilent Pmod peripheral modules. Pmods are small I/O interfaces, which connect with the embedded control boards through either 6- or 12-pin connectors. The PSoC Pioneer Kit supports the 6-pin Pmod type 2 (SPI) interface. For Digilent Pmod cards, go to www.digilentinc.com.

This header is not populated on the PSoC 4 Pioneer Kit. You must populate this header before connecting the Pmod daughter cards. Refer to the “No Load Components” section of A.6 Bill of Materials (BOM) on page 108 for the header part number.

Figure 4-10. Pmod Connection
Figure 4-11. Digilent Pmod Interface

See A.2 Pin Assignment Table on page 104 for details on the pin descriptions for the J5 header.

4.3.7 PSoC 5LP GPIO Header (J8)

A limited set of PSoC 5LP pins are brought to this header. Refer to 6.3 Developing Applications for PSoC 5LP on page 84 for details on how to develop custom applications. See A.2 Pin Assignment Table on page 104 for pin details.

Figure 4-12. PSoC 5LP GPIO Header (J8)
4.3.8 CapSense Slider

The kit has a five-segment linear capacitive touch slider on the board, which is connected to pins P1[1] to P1[5] of the PSoC 4 device.

The modulation capacitor (Cmod) is connected to pin P4[2] and an optional bleeder resistor (R1) can be connected across the Cmod. This board supports CapSense designs that enable waterproofing.

The waterproofing design uses a concept called shield, which is a conductor placed around the sensors. This shield must be connected to a designated shield pin on the device to function. The shield must be connected to the ground when not used. On the PSoC 4 Pioneer Kit, the connection of the shield to the pin or to the ground is made by resistors R44 and R45, respectively. By default, R45 is mounted on the board, which connects the shield to the ground. Populate R44 when evaluating waterproofing designs, which will connect the shield to the designated pin, P0[1]. This shield is different from the Arduino shields, which are boards that connect over the Arduino header. Refer to the CapSense Design Guide for further details related to CapSense.

Figure 4-13. CapSense Slider

Figure 4-14. CapSense Slider Connection
4.3.9 Pioneer Board LEDs

The PSoC 4 Pioneer board has three LEDs. A green LED (D10) indicates the status of the programmer. See A.5 Error in Firmware/Status Indication in Status LED for a detailed list of LED indications. An amber LED (D3) indicates status of power supplied to the board. The kit also has a general-purpose tricolor LED (D9) for user applications that connect to specific PSoC 4 pins.

Figure 4-15 shows the indication of all these LEDs on the board. Figure 4-16 and Figure 4-17 detail the LED schematic.

Figure 4-15. Pioneer Kit LEDs

![Pioneer Kit LEDs Diagram](image)

Figure 4-16. Status LED and Power LED

![Status LED and Power LED Diagram](image)

Figure 4-17. RGB LED

![RGB LED Diagram](image)
4.3.10 Push Buttons

The kit contains a Reset push button and a User push button, as shown in Figure 4-18.

The Reset button is connected to the XRES pin of PSoC 4 and is used to reset the onboard PSoC 4 device. The User button is connected to P0[7] of PSoC 4 device. Both the push buttons connect to ground on activation (active low).

Figure 4-18. Push Buttons
5. Code Examples

The code examples described in this chapter introduce the functionality of the PSoC 4 device and the onboard components. To access the examples, download the CD ISO image or setup files from the kit web page. The code examples will be available in the firmware folder in the install location.

Follow these steps to open and program code examples:
1. Launch PSoC Creator from the Start menu.
2. Open the code example by clicking `<Project.cywrk>` below Examples and Kits > Find Example Project > Kits > CY8CKIT-042.

Figure 5-1. Open Code Example from PSoC Creator
3. Build the code example by clicking **Build > Build <Project name>** to generate the hex file.

**Figure 5-2. Build Project from PSoC Creator**

![Figure 5-2. Build Project from PSoC Creator](image)

4. To program, connect the board to a computer using the USB cable connected to port J10, as described in section **3.1 Pioneer Kit USB Connection**. The board is detected as **KitProg**.

5. Click **Debug > Program** from PSoC Creator.

**Figure 5-3. Program Device from PSoC Creator**

![Figure 5-3. Program Device from PSoC Creator](image)

6. If the device is not yet acquired, PSoC Creator will open the programming window. Select **KitProg/** and click the **Port Acquire** button.

**Figure 5-4. Acquire Device from PSoC Creator**

![Figure 5-4. Acquire Device from PSoC Creator](image)
7. After the device is acquired, it is shown in a tree structure below the **KitProg**. Now, click the **Connect** button.

Figure 5-5. Connect Device from PSoC Creator

8. Click **OK** to exit the window and start programming.

Figure 5-6. Program Device from PSoC Creator
5.1 **Project: Blinking LED**

5.1.1 **Project Description**

This example uses a pulse-width modulator (PWM) to illuminate the RGB LED. The PWM output is connected to pin P0_3 (blue) of the RGB LED. The frequency of blinking is set to 1 Hz with a duty cycle of 50 percent. The blinking frequency and duty cycle can be varied by varying the period and compare value respectively.

**Note:** The PSoC 4 Pioneer Kit is factory-programmed with this example.

Figure 5-7. PSoC Creator Schematic Design of Blinking LED Project

5.1.2 **Hardware Connections**

No specific hardware connections are required for this project because all connections are hard-wired on the board. Open Blinking LED.cydwr in the Workspace Explorer and select the suitable pin.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Port Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>P0_3 (Blue)</td>
</tr>
</tbody>
</table>
5.1.3 Flow Chart

Figure 5-7 shows the flow chart of code implemented in `main.c`.

Figure 5-9. Blinking LED Project Flow Chart

5.1.4 Verify Output

Build and program the code example onto the device. Observe the frequency and duty cycle of the blinking LED. Change the period and compare value in the PWM component, as shown in Figure 5-10. Rebuild and reprogram the device to vary the frequency and duty cycle.
Figure 5-10. PWM Component Configuration Window
5.2 Project: PWM

5.2.1 Project Description

This code example demonstrates the use of the PWM component. The project uses three PWM outputs to set the color of RGB LED on the Pioneer Kit. The LED cycles through seven colors – violet > indigo > blue > green > yellow > orange > red (VIBGYOR). Each color is maintained for a duration of one second. The different colors are achieved by changing the pulse width of the PWMs.

Figure 5-11. PSoC Creator Schematic Design of PWM Project

5.2.2 Hardware Connections

No specific hardware connections are required for this project because all connections are hard-wired on the board. Open PWM.cydwr in the Workspace Explorer and select the suitable pins.

Table 5-2. Pin Connections

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Port Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM1</td>
<td>P1_6 (Red)</td>
</tr>
<tr>
<td>PWM2</td>
<td>P0_2 (Green)</td>
</tr>
<tr>
<td>PWM3</td>
<td>P0_3 (Blue)</td>
</tr>
</tbody>
</table>
5.2.3 Flow Chart

Figure 5-13 shows the flow chart of code implemented in main.c.

Figure 5-13. PWM Project Flow Chart

Start

Initialize the colormap for VIBGYOR

Initialize and start the PWM components

Wait for one second

Set the PWM widths to get next color in the color map
5.2.4 Verify Output

Build and program the code example, and reset the device. Observe the RGB LED cycles through the color pattern.

5.3 Project: Deep Sleep

5.3.1 Project Description

This project demonstrates the low-power functionality of the PSoC 4. The LED is turned on for one second to indicate Active mode; then, the device enters Deep-Sleep mode. When switch SW2 is pressed, the device wakes up and the LED is turned on for one second and then goes back into Deep-Sleep mode.

Figure 5-14. PSoC Creator Schematic Design of Deep-Sleep Project

5.3.2 Hardware Connections

No extra connections are required for the project functionality because the connections are hard-wired onto the board. To make low-power measurements using this project, refer to the use case detailed in section 4.3.3.2 Procedure to Measure PSoC 4 Current Consumption on page 34.

Open Deep Sleep.cydwr in the Workspace Explorer and select the suitable pin.

Table 5-3. Pin Connection

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Port Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED</td>
<td>P1_6 (Red)</td>
</tr>
<tr>
<td>Switch</td>
<td>P0_7</td>
</tr>
</tbody>
</table>
5.3.3 Flow Chart

Figure 5-15 shows the flow chart of code implemented in *main.c*. 

Figure 5-16. Deep-Sleep Project Flow Chart

1. Start
2. Turn LED on for one second
3. Enter Deep-Sleep mode
4. Interrupt on SW2 press
5. Clear the interrupt
5.3.4 Verify Output

Build and program the code example, and reset the device. LED is on for one second and turns off, which indicates that the device has entered Deep-Sleep mode. Press SW2 switch to wake up the device from Deep-Sleep mode and enter Active mode. The device goes back to sleep after one second.

**Note:** When the device is in Deep-Sleep mode, the programmer must reacquire the device before programming can start.

5.4 Project: CapSense

This code example can be executed in two ways – with and without CapSense tuning. The same project can be used to demonstrate the CapSense functionality as well as CapSense tuning using the Tuner Helper GUI in PSoC Creator. This is done by commenting and uncommenting the line `#define ENABLE_TUNING` in the `main.c` file of the code example. PSoC Creator does not compile the code under the `#ifdef (if defined)` statement when the `#define` statement is commented (/*……*/ or //). Similarly, when the `#define` statement is uncommented, the code required for working with Tuner GUI is compiled. By default, the project is set to work without CapSense tuning by commenting the `#define`.

5.4.1 CapSense (Without Tuning)

5.4.1.1 Project Description

This code example demonstrates CapSense on PSoC 4. The example uses the five-segment CapSense slider on the board. Each capacitive sensor on the slider is scanned using Cypress’s CapSense Sigma Delta (CSD) algorithm implemented in the CapSense component. This project is pre-tuned to take care of the board parasitics. For more information on the CapSense component and CapSense tuning, see the CapSense component datasheet in PSoC Creator.

In this code example, the brightness of the green and red LEDs are varied, based on the position of the user’s finger on the CapSense slider.

Figure 5-17. PSoC Creator Schematic Design of CapSense Project

**Note:** The EzI2C component is not used when tuning is disabled.
5.4.1.2 **Hardware Connections**

No specific hardware connections are required for this project because all connections are hard-wired on the board. Open `CapSense.cydwr` in the Workspace Explorer and select the suitable pins.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Port Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>CapSense linear slider</td>
<td>P1_1 Segment1</td>
</tr>
<tr>
<td></td>
<td>P1_2 Segment2</td>
</tr>
<tr>
<td></td>
<td>P1_3 Segment3</td>
</tr>
<tr>
<td></td>
<td>P1_4 Segment4</td>
</tr>
<tr>
<td></td>
<td>P1_5 Segment5</td>
</tr>
<tr>
<td>LEDs</td>
<td>P1_6 (Red) and P0_2 (Green)</td>
</tr>
<tr>
<td>I2C communication lines</td>
<td>P3_0 (SCL) and P3_1 (SDA)</td>
</tr>
</tbody>
</table>

**Note:** The I2C communication lines are not used when tuning is disabled.

Figure 5-18. Pin Selection for CapSense Project
5.4.1.3 Flow Chart

Figure 5-19 shows the flow chart of code implemented in main.c.

Figure 5-19. CapSense Project Flow Chart

5.4.1.4 Verify Output

The brightness of the green and red LEDs are varied based on the position of the user’s finger on the CapSense slider. When the finger is on segment 5 (P1[5]) of the slider, the green LED is brighter than the red LED; when the finger is on segment 1 (P1[1]) of the slider, the red LED is brighter than the green LED.

5.4.2 CapSense (With Tuning)

5.4.2.1 Project Description

This code example demonstrates CapSense tuning on PSoC 4 using the "Tuner" to monitor CapSense outputs. The CapSense outputs such as rawcounts, baseline, and signal (difference count) can be monitored on the Tuner GUI. The project uses the auto-tuning feature, which sets all CapSense parameters to the optimum values automatically. The parameter settings can be monitored in the GUI but cannot be altered. In the manual tuning method, parameter settings can be changed in the GUI and the resulting output can be seen.

The code example uses the five-segment CapSense slider on the board. Each capacitive sensor on the slider is scanned using Cypress's CapSense Sigma Delta (CSD) algorithm implemented in the CapSense component. The code uses tuner APIs. The tuner API CapSense_TunerComm() is used in the main loop to scan sensors, which also sends the CapSense variables RawCounts, Baseline, and Difference Counts (Signal) to the PC GUI through I2C communication.
In this example, the brightness of the green and red LEDs are varied, based on the position of the user's finger on the CapSense slider.

See Figure 5-17 for the project schematic.

**5.4.2.2 Hardware Connections**

No specific hardware connections are required for this project because all connections are hard-wired on the board. Open CapSense.cydwr in the Workspace Explorer and select the suitable pins. See Table 5-4 and Figure 5-18 for the CapSense project pin connections.

**5.4.2.3 Flow Chart**

![Flow Chart](image)

Start

- Initialise and start the PWM and CapSense Tuner

- Start Tuner communication

- Get the finger position on the slider

- Set the PWM output width to adjust the brightness of the RGB LED
5.4.2.4 Launching Tuner GUI

The Tuner GUI from PSoC Creator should be up and running for the code example to work. To launch the GUI follow these steps:

1. Go to the project’s TopDesign.cysch file.

Figure 5-21. Top Design File

2. To open the tuner, right-click on the CapSense_CSD component in PSoC Creator and click Launch Tuner.

Figure 5-22. Launch Tuner

3. The Tuner GUI opens. Click Configuration to open the configuration window.
4. Set the I2C communication parameters, as shown in the following figure.

Figure 5-24. I2C Communication
5. Click **OK** to apply the settings.

5.4.2.5 **Verify Output**

1. To start the scanning and communication process, click **Start**.

Figure 5-25. Start Communication
2. Select a sensor in the Tuning tab. A red outline is seen on the selected sensor. Different CapSense parameters are shown on the bottom-right. You cannot edit the settings because auto-tuning is used in this project; auto-tuning automatically sets all the parameters. Touch the selected sensor and observe the response in the tuner window.

Figure 5-26. Sensor Tuning

3. In the Graphing tab, the CapSense results: Raw counts, Baseline, Signal (difference count) and On/Off status for each sensor are represented as a graph.

4. Select the sensor parameters to observe, as shown in the following figure. The graph of the selected parameters is shown.
Figure 5-27. Sensor Parameter Graph
5. Touch a sensor or slider element and see the increase in raw counts.

Figure 5-28. Raw Count Increase
6. Advanced Topics

6.1 Using PSoC 5LP as USB-UART Bridge

The PSoC 5LP serves as a USB-UART bridge, which can communicate with the COM terminal software. This section explains how to create a PSoC 4 code example to communicate with the COM terminal software. This project is available with other code examples for the PSoC 4 Pioneer Kit at the element14 web page, 100 Projects in 100 days.

Users who have a Windows operating system that does not have HyperTerminal can use an alternate terminal software such as PuTTY.

1. Open a new PSoC 4 project in the PSoC Creator. Select an appropriate location for your project and rename the project as required.

Figure 6-1. Opening New Project from PSoC Creator
2. Drag and drop a UART (SCB) component to the top design.

Figure 6-2. UART Component Under Component Catalog

3. To configure the UART, double-click or right-click on the UART component and select **Configure**.

Figure 6-3. Open UART Configuration Window
4. Configure the UART as shown in the following figures.

Figure 6-4. UART Configuration Window

![UART Configuration Window](image)

Figure 6-5. UART Basic Configuration Window

![UART Basic Configuration Window](image)
6. Place the following code in your main.c project file. The code will echo any UART data received.

```c
int main()
{
    uint8 ch;
    /* Start SCB UART TX+RX operation */
    UART_Start();

    /* Transmit String through UART TX Line */
    UART_UartPutString("CY8CKIT-042 USB-UART");
    for(;;)
    {
        /* Get received character or zero if nothing has been received yet */
        ch = UART_UartGetChar();
        if(0u != ch)
        {
            /* Send the data through UART. This function is blocking and waits until there is an entry into the TX FIFO. */
            UART_UartPutChar(ch);
        }
    }
}
```
7. Build the project by clicking **Build > Build {Project Name}** or **[Shift] + [F6]**. After the project is built without errors and warnings, program (by clicking **Debug > Program**) the project to PSoC 4 through the PSoC 5LP USB programmer or MiniProg3.

Connect the RX line of the PSoC 4 to J8_10 and TX line of the PSoC 4 to J8_9, as shown in the following figures.

**Figure 6-8. UART Connection Between PSoC 4 and PSoC 5LP**

![UART Connection Between PSoC 4 and PSoC 5LP](image)

**Figure 6-9. Block Diagram of UART Connection Between PSoC 4 and PSoC 5LP**

![Block Diagram of UART Connection Between PSoC 4 and PSoC 5LP](image)

**Note:** UART RX and UART TX can be routed to any digital pin on PSoC 4 based on the configuration of the UART component. An SCB implementation of UART will route the RX and TX pins to either one of the following subsets: (P0[4], P0[5]) or (P3[0], P3[1]) or (P4[0], P4[1]).
To communicate with the PSoC 4 from the terminal software, follow this procedure:
1. Connect USB Mini B to J10. The kit enumerates as a KitProg USB-UART and is available under the Device Manager, Ports (COM & LPT). A communication port is assigned to the KitProg USB-UART.

2. Open HyperTerminal and select **File > New Connection** and enter a name for the new connection and click **OK**.
   For PuTTY, double click the putty icon and select **Serial** under **Connection**.
Figure 6-11. Open New Connection

HyperTerminal

3. A new window opens, where the communication port can be selected.
   In HyperTerminal, select COMX (or the specific communication port that is assigned to KitProg USB-UART) in **Connect using** and click **OK**.
   In PuTTY enter the COMX in **Serial line to connect to**.
   This code example uses **COM12**.
4. In HyperTerminal, select 'Bits per second', 'Data bits', 'Parity', 'Stop bits', and 'Flow control' under Port Settings and click OK.

Make sure that the settings are identical to the UART settings configured for PSoC 4.

In PuTTY select 'Speed (baud)', 'Data bits', 'Stop bits', 'Parity' and 'Flow control' under Configure the serial line. Click Session and select Serial under Connection type.
**Serial line** shows the communication port (COM12) and **Speed** shows the baud rate selected. Click **Open** to start the communication.

Figure 6-13. Configure the Communication Port

**HyperTerminal**

![HyperTerminal Configuration](image)

**PuTTY**

![PuTTY Configuration](image)
5. Enable **Echo typed characters locally** under *File > Properties > Settings > ASCII Setup*, to display the typed characters on HyperTerminal. In PuTTY, enable the **Force on** under *Terminal > Line discipline* options to display the typed characters on the PuTTY.

![Select Communication Type in PuTTY](image)

**Figure 6-14.** Select Communication Type in PuTTY

![Enabling echo of typed characters in HyperTerminal](image)

**Figure 6-15.** Enabling echo of typed characters in HyperTerminal
6. The COM terminal software displays both the typed data and the looped back data from the PSoC 4 UART.

Figure 6-17. Data Displayed on HyperTerminal
Figure 6-18. Data Displayed on PuTTY
6.2 Using PSoC 5LP as USB-I2C Bridge

The PSoC 5LP serves as a USB-I2C bridge, which can be used to communicate with the USB-I2C software running on the PC. This project is available with other code examples for the PSoC 4 Pioneer Kit at the element14 web page, 100 Projects in 100 days.

The following steps describe how to use the USB-I2C bridge, which can communicate between the BCP and the PSoC 4.

1. Open a new project targeting the PSoC 4 device in PSoC Creator.

Figure 6-19. Opening a New Project in PSoC Creator
2. Drag and drop an I2C component to the top design.

Figure 6-20. I2C Component in Component Catalog

3. To configure the I2C component, double-click or right-click on the I2C component and select Configure.

Figure 6-21. Open I2C Configuration Window
4. Configure the I2C with the following settings.

Figure 6-22. I2C Configuration Tab

Figure 6-23. I2C Tab

5. Select pin P3[0] for the I2C SCL and pin P3[1] for the I2C SDA in the Pins tab of `<project.cydwr>`.
6. Place the following code in your `main.c` project file. The code will enable the PSoC 4 device to transmit and receive I2C data to and from the BCP application.

```c
int main()
{

    uint8 wrBuf[10];    /* I2C write buffer */
    uint8 rdBuf[10];    /* I2C read buffer */
    uint8 indexCntr;
    uint32 byteCnt;

    /* Enable the Global Interrupt */
    CyGlobalIntEnable;

    /* Start I2C Slave operation */
    I2C_Start();

    /* Initialize write buffer */
    I2C_I2CSlaveInitWriteBuf((uint8 *) wrBuf, 10);

    /* Initialize read buffer */
    I2C_I2CSlaveInitReadBuf((uint8 *) rdBuf, 10);

    for(;;) /* Loop forever */
    {

        /* Wait for I2C master to complete a write */
```
if(0u != (I2C_I2CSlaveStatus() & I2C_I2C_SSTAT_WR_CMPLT))
{
    /* Read the number of bytes transferred */
    byteCnt = I2C_I2CSlaveGetWriteBufSize();

    /* Clear the write status bits*/
    I2C_I2CSlaveClearWriteStatus();

    /* Move the data written by the master to the read buffer so that the
     master can read back the data */
    for(indexCntr = 0; indexCntr < byteCnt; indexCntr++)
    {
        rdBuf[indexCntr] = wrBuf[indexCntr]; /* Loop back the data to the read
        buffer */
    }

    /* Clear the write buffer pointer so that the next write operation will
     start from index 0 */
    I2C_I2CSlaveClearWriteBuf();

    /* Clear the read buffer pointer so that the next read operations starts
     from index 0 */
    I2C_I2CSlaveClearReadBuf();

    /* If the master has read the data , reset the read buffer pointer to 0
     and clear the read status */
    if(0u != (I2C_I2CSlaveStatus() & I2C_I2C_SSTAT_RD_CMPLT))
    {
        /* Clear the read buffer pointer so that the next read operations starts
         from index 0 */
        I2C_I2CSlaveClearReadBuf();

        /* Clear the read status bits */
        I2C_I2CSlaveClearReadStatus();
    }
}

6. Build the project by clicking **Build > Build Project** or **[Shift]+[F6]**. After the project is built without
errors and warnings, program (**[Ctrl]+[F5]**) this code onto the PSoC 4 through the PSoC 5LP pro-
grammer or MiniProg3.

7. Open the BCP from **Start > All Programs > Cypress > Bridge Control Panel <version num-
ber>**.

8. Connect to **KitProg/** under **Connected I2C/SPI/RX8 Ports**.
9. Open **Protocol Configuration** from the **Tools** menu and select the appropriate **I2C Speed**. Make sure the I2C speed is the same as the one configured in the I2C component. Click **OK** to close the window.
10. From the BCP, transfer five bytes of data to the I2C device with slave address 0x08. The log shows whether the transaction was successful. A ‘+’ indication after each byte indicates that the transaction was successful and a ‘–’ indicates that the transaction was a failure.

Figure 6-27. Entering Commands in BCP
11. From the BCP, read five bytes of data from the I2C slave device with slave address 0x08. The log shows whether the transaction was successful.

**Figure 6-29. Read Data Bytes from the BCP**

*Note: Refer Help Contents under Help in BCP or press [F1] for details of I2C commands.*
6.3 Developing Applications for PSoC 5LP

The PSoC 4 Pioneer Kit has an onboard PSoC 5LP whose primary function is that of a programmer and a bridge. You can build either a normal project or a bootloadable project using the PSoC 5LP.

The PSoC 5LP connections in the Pioneer board are summarized in Figure 6-30. J8 is the I/O connector (see section 4.3.7 PSoC 5LP GPIO Header (J8)). The USB (J10) is connected and used as the PC interface. But you can still use this USB connection to create customized USB designs.

The programming header (J7) is meant for standalone programming. This header needs to be populated. See the 'No Load Components' section in A.6 Bill of Materials (BOM) on page 108.

Figure 6-30. PSoC 5LP Block Diagram

6.3.1 Building a Bootloadable Project for PSoC 5LP

All bootloadable applications developed for the PSoC 5LP should be based on the bootloader hex file, which is programmed onto the kit. The bootloader hex file is available in the kit files or can be downloaded from the kit web page.

The hex files are included in the following kit installer directory:
<Install Path>\CY8CKIT-042 PSoC 4 Pioneer Kit\<version>\Firmware\Programmer\KitProg_Bootloader

Figure 6-31. KitProg Bootloader Hex File Location

To build a bootloadable application for the PSoC 5LP, follow this procedure:
1. In PSoC Creator, select **New > Project > PSoC 5LP**; click the expand button adjacent to **Advanced** and select the **Device** as **CY8C5868LTI-LP043**, as shown in Figure 6-33. Select the **Application Type** as **Bootloadable** from the drop-down list.

Figure 6-32. Opening New Project in PSoC Creator
2. Navigate to the Schematic view and drag and drop a bootloadable component on the top design.

Figure 6-34. Bootloadable Component in Component Catalog
Set the dependency of the Bootloadable component by selecting the Dependencies tab in the configuration window and clicking the Browse button. Select the KitProg_Bootloader.hex and KitProg_Bootloader.elf files; click Open.

Figure 6-35. Configuration Window of Bootloadable Component

Figure 6-36. Selecting KitProg Bootloader Hex File
3. Develop your custom project.
4. The NVL setting of the Bootloadable project and the KitProg_Bootloader project must be the same. The KitProg_Bootloader.cydwr system settings is shown in the following figure.

5. Build the project in PSoC Creator by selecting **Build > Build Project** or **[Shift]+[F6]**.
6. To download the project on to the PSoC 5LP device, open the Bootloader Host Tool, which is available from PSoC Creator. Select **Tools > Bootloader Host**.

**Figure 6-39. Opening Bootloader Host Tool from PSoC Creator**

7. In the Bootloader Host tool, click **Filters** and add a filter to identify the USB device. Set VID as **0x04B4**, PID as **0xF13B**, and click **OK**.

**Figure 6-40. Port Filters Tab in Bootloader Host Tool**
8. In the Bootloader Host tool, click the **Open File** button to browse to the location of the bootloadable file (*.cyacd).

![Figure 6-41. Opening Bootloadable File from Bootloader Host Tool](image)

9. Keep the reset switch (SW1) pressed and plug in the USB Mini-B connector. If the switch is pressed for more than 100 ms, the PSoC 5LP enters into bootloader. Press the **Program** button in the Bootloader Host tool to program the device. The PSoC 5LP also enters into bootloader when the power supply jumper for the PSoC 4 (J13) is removed and subsequently the USB Mini-B connector is plugged into header J10.

![Figure 6-42. Selecting Bootloadable .cyacd File from Bootloader Host](image)
10. If bootload is successful, the log of the tool displays "Successful"; otherwise, it displays "Failed" and a statement for the failure.

Notes:
1. The PSoC 5LP pins are brought to the PSoC 5LP GPIO header (J8). These pins are selected to support high-performance analog and digital projects. See A.2 Pin Assignment Table on page 104 for pin information.
2. Take care when allocating the PSoC 5LP pins for custom applications. For example, P2[0]–P2[4] are dedicated for programming the PSoC 4. Refer to A.1 CY8CKIT-042 Schematics on page 101 before allocating the pins.
3. When a normal project is programmed onto the PSoC 5LP, the initial capability of the PSoC 5LP to act as a programmer, USB-UART bridge, or USB-I2C bridge is not available.
4. The status LED does not function unless used by the custom project.

For additional information on bootloaders, refer to Cypress application note, AN73503 - USB HID Bootloader for PSoC 3 and PSoC 5LP.
6.3.2 Building a Normal Project for PSoC 5LP

A normal project is a completely new project created for the PSoC 5LP device on the CY8CKIT-042. Here the entire flash of the PSoC 5LP is programmed, overwriting all bootloader and programming code. To recover the programmer, reprogram the PSoC 5LP device with the factory-set KitProg.hex file, which is shipped with the kit installer.

The KitProg.hex file is available at the following location:
<Install Path>/CY8CKIT-042 PSoC 4 Pioneer Kit\<version>\Firmware\Programmer\KitProg

This advanced functionality requires a MiniProg3 programmer, which is not included with this kit. The MiniProg3 can be purchased from www.cypress.com/go/CY8CKit-002.

To build a normal project for the PSoC 5LP, follow these steps:
1. In PSoC Creator, select New > Project > PSoC 5LP; click the expand button adjacent to Advanced and select Device as CY8C5868LTI-LP039; select Application Type as Normal from the drop-down list.

2. Develop your custom project.
3. Build the project in PSoC Creator by selecting Build > Build Project or [Shift]+[F6].
4. Connect the 10-pin connector of MiniProg3 to the onboard 10-pin SWD debug and programming header J7 (which needs to be populated).
5. To program the PSoC 5LP with PSoC Creator, click Debug > Program or [Ctrl]+[F5]. The Programming window shows MiniProg3 and the selected device in the project under it (CY8C5868LTI-LP039).
6. Click on the device and click **Connect** to program.

**Notes:**
1. The 10-pin SWD debug and programming header (J7) is not populated. See the 'No Load Components' section of **A.6 Bill of Materials (BOM)** for details.
2. The PSoC 5LP pins are brought to the PSoC 5LP GPIO header (J8). These pins are selected to support high-performance analog and digital projects. See **A.2 Pin Assignment Table** for pin information.
3. Take care when allocating the PSoC 5LP pins for custom applications. For example, P2[0]–P2[4] are dedicated for programming the PSoC 4. Refer to **A.1 CY8CKIT-042 Schematics** before allocating the pins.
4. When a normal project is programmed onto the PSoC 5LP, the initial capability of the PSoC 5LP to act as a programmer, USB-UART bridge, or USB-I2C bridge in not available.
5. The status LED does not function unless used by the custom project.

### 6.4 PSoC 5LP Factory Program Restore Instructions

The CY8CKIT-042 PSoC 4 Pioneer Kit features a PSoC 5LP device that comes factory-programmed as the onboard programmer and debugger for the PSoC 4 device.

In addition to creating applications for the PSoC 4 device, you can also create custom applications for the PSoC 5LP device on this kit. For details, see section **6.3 Developing Applications for PSoC 5LP** on page 84. Reprogramming or bootloading the PSoC 5LP device with a new flash image will overwrite the factory program and forfeit the ability to use the PSoC 5LP device as a programmer/debugger for the PSoC 4 device. Follow the instructions to restore the factory program on the PSoC 5LP and enable the programmer/debugger functionality.

#### 6.4.1 PSoC 5LP is Programmed with a Bootloadable Application

If the PSoC 5LP is programmed with a bootloaderable application, restore the factory program by using one of the following two methods.

**6.4.1.1 Restore PSoC 5LP Factory Program Using PSoC Programmer**

1. Launch **PSoC Programmer 3.18** or later from **Start > Cypress > PSoC Programmer**.
2. Configure the Pioneer Kit in Service Mode. To do this, while holding down the reset button (SW1 Reset), plug in the PSoC 4 Pioneer Kit to the computer using the included USB cable (USB A to mini-B). This puts the PSoC 5LP into service mode, which is indicated by the blinking green status LED.
3. The following message appears in the PSoC Programmer results window “KitProg Bootloader device is detected”.

Figure 6-44. PSoC Programmer Results Window

![PSoC Programmer Results Window](image)

4. Switch to the Utilities tab in PSoC Programmer and press the Upgrade Firmware button. Unplug all other PSoC programmers (such as MiniProg3 and DVKProg) from the PC before pressing the Upgrade Firmware button.

Figure 6-45. Upgrade Firmware

![Upgrade Firmware](image)
5. After programming has completed, the following message appears: “Firmware Update Finished at <time>”.

Figure 6-46. Firmware Update Complete

6. The factory program is now successfully restored on the PSoC 5LP. It can be used as the programmer/debugger for the PSoC 4 device.
6.4.1.2 *Restore PSoC 5LP Factory Program Using USB Host Tool*

1. Launch the Bootloader Host tool from **Start > Cypress > PSoC Creator**.

2. Using the **File > Open** menu, load the *Kit Prog.cyacd* file, which is installed with the kit software. The default location for this file is: `<Install Path>\CY8CKIT-042 PSoC 4 Pioneer Kit\<version>\Firmware\Programmer\KitProg\KitProg.cyacd`

![Figure 6-47. Load KitProg.cyacd File](image-url)
3. Configure the Pioneer Kit in Service Mode. To do this, while holding down the reset button (SW1 Reset), plug in the PSoC 4 Pioneer Kit to the computer using the included USB cable (USB A to mini-B). This puts the PSoC 5LP into service mode, which is indicated by the blinking green status LED.

4. In the Bootloader Host tool, set the filters for the USB devices with VID: 04B4 and PID: F13B. **USB Human Interface Device** port appears in the Ports list. Click that port to select it.

**Figure 6-48. Select USB Human Interface Device**

5. Click the **Program** button (or menu item **Actions > Program**) to restore the factory-program by bootloading it onto the PSoC 5LP.

6. After programming has completed, the following message appears: “Programming Finished Successfully”.

7. The factory program is now successfully restored on the PSoC 5LP. It can be used as the programmer/debugger for the PSoC 4 device.

6.4.2 PSoC 5LP is Programmed with a Standard Application

If PSoC 5LP is programmed with a standard application, restore the factory program by using the following method.

1. Launch **PSoC Programmer 3.18** or later from **Start > Cypress > PSoC Programmer**.
2. Use the **File > Open** menu to load the KitProg.hex factory program hex file, which is shipped with the kit. The default location for this file is: `<Install Path>\CY8CKIT-042 PSoC 4 Pioneer Kit\<version>\Firmware\Programmer\KitProg`
3. Connect a **CY8CKIT-002** MiniProg3 (sold separately) to the computer. The 10-pin connector cable on the MiniProg3 plugs into the header [J7]. Note that the J7 header is unpopulated. For more details, see **A.6 Bill of Materials (BOM) on page 108.**
4. Ensure that **MiniProg3** is the selected port in PSoC Programmer and the 10-pin connector (10p option) is selected, as shown in the following figure. If the board is not powered over USB, select the **Power Cycle** programming mode.

Figure 6-50. Select MiniProg3

5. When ready, press the **Program** button (or **File > Program**) to program the PSoC 5LP device.

6. After programming has completed, the following message appears: “Program Finished at <time>”.
7. The factory program is now successfully restored on the PSoC 5LP. It can be used as the programmer/debugger for the PSoC 4 device.
A. Appendix

A.1 CY8CKIT-042 Schematics

Power Supply
Input Voltage Range VIN is 5-12V

USB MiniB

PTC Releasable Fuse
## A.2 Pin Assignment Table

This section provides the pin map of the headers and their usage.

### A.2.1 Arduino Compatible Headers (J1, J2, J3, J4, and J12)

#### J1

<table>
<thead>
<tr>
<th>Pin</th>
<th>Kit Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1_01</td>
<td>VIN</td>
<td>Input voltage to the board</td>
</tr>
<tr>
<td>J1_02</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>J1_03</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>J1_04</td>
<td>5V</td>
<td>5 V voltage</td>
</tr>
<tr>
<td>J1_05</td>
<td>3.3V</td>
<td>3.3 V voltage</td>
</tr>
<tr>
<td>J1_06</td>
<td>RESET</td>
<td>/XRES</td>
</tr>
<tr>
<td>J1_07</td>
<td>IOREF</td>
<td>I/O voltage reference</td>
</tr>
<tr>
<td>J1_08</td>
<td>NC</td>
<td>Not connected</td>
</tr>
</tbody>
</table>

#### J2

<table>
<thead>
<tr>
<th>Pin</th>
<th>PSoC 4 Signal</th>
<th>PSoC 4 Description</th>
<th>Pin</th>
<th>PSoC 4 Signal</th>
<th>PSoC 4 Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2_01</td>
<td>P2[0]</td>
<td>A0 (SARADC input)</td>
<td>J2_02</td>
<td>P0[2]</td>
<td>Comparator 2+</td>
</tr>
<tr>
<td>J2_05</td>
<td>P2[2]</td>
<td>A2 (SARADC input)</td>
<td>J2_06</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>J2_13</td>
<td>P0[0]</td>
<td>Comparator 1+</td>
<td>J2_14</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>J2_17</td>
<td>P1[0]</td>
<td>Opamp 1+</td>
<td>J2_18</td>
<td>P1[1]</td>
<td>Opamp 1–</td>
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</table>

#### J3

<table>
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<th>Pin</th>
<th>PSoC 4 Signal</th>
<th>PSoC 4 Description</th>
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</thead>
<tbody>
<tr>
<td>J3_01</td>
<td>P2[6]</td>
<td>D8</td>
</tr>
<tr>
<td>J3_02</td>
<td>P3[6]</td>
<td>D9(PWM)</td>
</tr>
<tr>
<td>J3_03</td>
<td>P3[4]</td>
<td>D10(PWM/SS)</td>
</tr>
<tr>
<td>J3_04</td>
<td>P3[0]</td>
<td>D11(PWM/MOSI)</td>
</tr>
<tr>
<td>J3_05</td>
<td>P3[1]</td>
<td>D12(MISO)</td>
</tr>
<tr>
<td>J3_06</td>
<td>P0[6]</td>
<td>D13(SCK)</td>
</tr>
<tr>
<td>J3_07</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>J3_08</td>
<td>P1[7]</td>
<td>AREF</td>
</tr>
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<td>J3_09</td>
<td>P4[1]</td>
<td>SDA</td>
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<td>J3_10</td>
<td>P4[0]</td>
<td>SCL</td>
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<th>Pin</th>
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<th>PSoC 4 Description</th>
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</thead>
<tbody>
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<td>J4_01</td>
<td>P0[4]</td>
<td>D0(RX)</td>
</tr>
<tr>
<td>J4_02</td>
<td>P0[5]</td>
<td>D1(TX)</td>
</tr>
<tr>
<td>J4_03</td>
<td>P0[7]</td>
<td>D2</td>
</tr>
<tr>
<td>J4_04</td>
<td>P3[7]</td>
<td>D3(PWM)</td>
</tr>
<tr>
<td>J4_05</td>
<td>P0[0]</td>
<td>D4</td>
</tr>
<tr>
<td>J4_06</td>
<td>P3[5]</td>
<td>D5(PWM)</td>
</tr>
<tr>
<td>J4_07</td>
<td>P1[0]</td>
<td>D6(PWM)</td>
</tr>
<tr>
<td>J4_08</td>
<td>P2[7]</td>
<td>D7</td>
</tr>
</tbody>
</table>

### J12

<table>
<thead>
<tr>
<th>Pin</th>
<th>Kit Signal</th>
<th>PSoC 4 Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J12_01</td>
<td>P3[1]</td>
<td>MISO</td>
</tr>
<tr>
<td>J12_02</td>
<td>PSoc 4_VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>J12_03</td>
<td>P0[6]</td>
<td>SCK</td>
</tr>
<tr>
<td>J12_04</td>
<td>P3[0]</td>
<td>MOSI</td>
</tr>
<tr>
<td>J12_05</td>
<td>/XRES</td>
<td>PSoc 4 RESET</td>
</tr>
<tr>
<td>J12_06</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

### A.2.2 Digilent Pmod Cards Support Header (J5)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Kit Signal</th>
<th>PSoC 4 Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5_01</td>
<td>P3[5]</td>
<td>SPI_SS (multiplex with J4_06)</td>
</tr>
<tr>
<td>J5_02</td>
<td>P3[0]</td>
<td>SPI_MOSI</td>
</tr>
<tr>
<td>J5_03</td>
<td>P3[1]</td>
<td>SPI_MISO</td>
</tr>
<tr>
<td>J5_04</td>
<td>P0[6]</td>
<td>SPI_SCK</td>
</tr>
<tr>
<td>J5_05</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>J5_06</td>
<td>VDD</td>
<td>VCC</td>
</tr>
</tbody>
</table>
A.2.3 **PSoC 5LP GPIO Header (J8)**

J8 is a 2×6 header that connects PSoC 5LP pins to support GPIO controls for custom PSoC 5LP projects.

<table>
<thead>
<tr>
<th>J8</th>
<th>Pin</th>
<th>PSoC 5LP Signal</th>
<th>PSoC 5LP Description</th>
<th>Pin</th>
<th>PSoC 5LP Signal</th>
<th>PSoC 5LP Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J8_01</td>
<td>PSoC 5LP_VDD</td>
<td>VDD</td>
<td></td>
<td>J8_02</td>
<td>P1[2]</td>
<td>Digital I/O</td>
</tr>
<tr>
<td>J8_03</td>
<td>P0[0]</td>
<td>Delta Sigma ADC + input</td>
<td>J8_04</td>
<td>P0[1]</td>
<td>Delta Sigma ADC – input</td>
<td></td>
</tr>
<tr>
<td>J8_11</td>
<td>GND</td>
<td>GND</td>
<td>J8_12</td>
<td>P3[0]</td>
<td>IDAC output</td>
<td></td>
</tr>
</tbody>
</table>

**A.3 Program and Debug Headers**

A.3.1 **PSoC 4 Direct Program/Debug Header (J6)**

<table>
<thead>
<tr>
<th>J6</th>
<th>Pin</th>
<th>PSoC 5LP Signal</th>
<th>PSoC 4 Signal</th>
<th>Description</th>
<th>Pin</th>
<th>PSoC 5LP Signal</th>
<th>PSoC 4 Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J6_01</td>
<td>VDD</td>
<td>VDD</td>
<td>VCC</td>
<td>J6_02</td>
<td>P2[0]</td>
<td>P3[2]</td>
<td>TMS/SWDIO</td>
<td></td>
</tr>
<tr>
<td>J6_05</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>J6_06</td>
<td>P2[2]</td>
<td>NC</td>
<td>TDO/SWO</td>
<td></td>
</tr>
<tr>
<td>J6_07</td>
<td>NC</td>
<td>GND</td>
<td>GND</td>
<td>J6_08</td>
<td>P2[3]</td>
<td>NC</td>
<td>TDI</td>
<td></td>
</tr>
</tbody>
</table>

A.3.2 **PSoC 5LP Direct Program/Debug Header (J7)**

<table>
<thead>
<tr>
<th>J7</th>
<th>Pin</th>
<th>PSoC 5LP Signal</th>
<th>Description</th>
<th>Pin</th>
<th>PSoC 5LP Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7_01</td>
<td>VDD</td>
<td>VCC</td>
<td>J7_02</td>
<td>P1[0]</td>
<td>TMS/SWDIO</td>
<td></td>
</tr>
<tr>
<td>J7_03</td>
<td>GND</td>
<td>GND</td>
<td>J7_04</td>
<td>P1[1]</td>
<td>TCLK/SWCLK</td>
<td></td>
</tr>
<tr>
<td>J7_05</td>
<td>GND</td>
<td>GND</td>
<td>J7_06</td>
<td>P1[3]</td>
<td>TDO/SWO</td>
<td></td>
</tr>
<tr>
<td>J7_07</td>
<td>GND</td>
<td>GND</td>
<td>J7_08</td>
<td>P1[4]</td>
<td>TDI</td>
<td></td>
</tr>
<tr>
<td>J7_09</td>
<td>GND</td>
<td>GND</td>
<td>J7_10</td>
<td>XRES</td>
<td>RESET</td>
<td></td>
</tr>
</tbody>
</table>
A.4 Use of Zero-ohm Resistors and No Load

<table>
<thead>
<tr>
<th>Unit</th>
<th>Resistor</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>R2</td>
<td>Solder zero-ohm resistors to access voltage from VBUS (USB).</td>
</tr>
<tr>
<td>I2C connection between PSoC 5LP and PSoC 4</td>
<td>R24 and R25</td>
<td>Unsolder the resistors to communicate with an external PSoC using the PSoC 5LP. Removing these will disable the PSoC 4 programming by the PSoC 5LP device.</td>
</tr>
<tr>
<td>PSoC 4/external PSoC program/debug header</td>
<td>R32, R33, and R34</td>
<td>Unsolder the resistors to disconnect SWD lines from the PSoC 4. Use J6 to connect and program an external PSoC.</td>
</tr>
<tr>
<td>Protection circuit</td>
<td>R46</td>
<td>Solder zero-ohm resistors to bypass the entire protection circuitry.</td>
</tr>
<tr>
<td>CapSense tuning circuitry</td>
<td>R1</td>
<td>Used when RBleed mode of the CSD is used. To use this feature, you must populate an RBleed resistor. Refer to the CapSense component datasheet.</td>
</tr>
<tr>
<td>CapSense shield setting</td>
<td>R44, R45</td>
<td>Unsolder R45, which connects the shield to ground and solder R44 with zero-ohm resistors to connect Vref via P0_1.</td>
</tr>
<tr>
<td>PSoC 4</td>
<td>R4, R6</td>
<td>Unsolder R4 to remove supply to VTARG and solder zero-ohm resistors R6 to supply P4_VDD with VDD instead of J13.</td>
</tr>
<tr>
<td>PSoC 5LP programmer/debugger</td>
<td>R11, R12, R14, R15, R16</td>
<td>For future use.</td>
</tr>
<tr>
<td>R5</td>
<td>Unsold er the zero-ohm resistor to cut the VDD supply to PSoC 5LP.</td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td>For future use.</td>
<td></td>
</tr>
</tbody>
</table>

A.5 Error in Firmware/Status Indication in Status LED

<table>
<thead>
<tr>
<th>User Indication</th>
<th>Scenario</th>
<th>Action Required by user</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 LED blinks at a fast rate (ON Time = 0.25s, OFF Time = 0.25s)</td>
<td>Bootloadable file is corrupt</td>
<td>Bootload the *.cyacd file over the USB interface, which is shipped with PSoC Programmer using the Bootloader Host GUI shipped with PSoC Creator. The files are located in the PSoC Programmer root installation directory.</td>
</tr>
</tbody>
</table>
| 2 LED blinks at a slow rate (ON Time = 1.5s, OFF Time = 1.5s) | Entered Bootloader by pressing the PSoC 4 Reset switch | a) Unplug power and plug it in again if you entered this mode by mistake; the LED gives the indication.  
b) If the mode entry was intentional, bootload the new *.cyacd file using the Bootloader Host tool shipped with PSoC Creator. |
| 3 LED glows steadily | Programmer application is running successfully | USB is enumerated successfully and the programmer is up and running. The PSoC 4 device can now be programmed any time using the onboard PSoC 5LP programmer. |

**Note:** LED status is not applicable when a custom project is running in PSoC 5LP.
### A.6 Bill of Materials (BOM)

<table>
<thead>
<tr>
<th>No.</th>
<th>Qty</th>
<th>Reference</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Mfr Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>PCB, 3.32&quot;x2.1&quot; CAF resistant High Tg ENIG finish, 4 layer, Color = RED, Silk = WHITE.</td>
<td>Cypress</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>C1</td>
<td>2200 pF</td>
<td>CAP CER 2200PF 50V 5% NP0 0805</td>
<td>Murata</td>
<td>GRM2165C1H222JA01D</td>
</tr>
<tr>
<td>3</td>
<td>12</td>
<td>C2,C7,C12,C14,C15,C17,C20,C21,C22,C24,C25,C27</td>
<td>0.1 uF</td>
<td>CAP .1UF 16V CERAMIC Y5V 0402</td>
<td>Panasonic - ECG</td>
<td>ECJ-0EF1C104Z</td>
</tr>
<tr>
<td>4</td>
<td>11</td>
<td>C3,C5,C8,C10,C11,C13,C18,C19,C23,C26,C28</td>
<td>1.0 uF</td>
<td>CAP CERAMIC 1.0UF 25V X5R 0603 10%</td>
<td>Taiyo Yuden</td>
<td>TMY107BJ105KA-T</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>C4</td>
<td>10 uF 25V</td>
<td>CAP TANT 10UF 25V 10% 1210</td>
<td>AVX Corporation</td>
<td>TPSB106K025R1800</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>C6</td>
<td>22 uF 16V</td>
<td>CAP TANT 22UF 16V 10% 1210</td>
<td>AVX Corporation</td>
<td>TPSB226K016R0600</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>C9</td>
<td>10000 pF</td>
<td>CAP CER 10000PF 50V 5% NP0 0805</td>
<td>Murata</td>
<td>GRM2195C1H103JA01D</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>C16</td>
<td>0.01 uF</td>
<td>CAP 10000PF 16V CERAMIC 0402 SMD</td>
<td>Panasonic - ECG</td>
<td>ECJ-0EB1C103K</td>
</tr>
<tr>
<td>9</td>
<td>6</td>
<td>D1,D2,D4,D11,D12,D13</td>
<td>MBR05</td>
<td>DIODE SCHOTTKY 0.5A 20V SOD-123</td>
<td>Fairchild Semiconductor</td>
<td>MBR0520L</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>D3</td>
<td>Power LED Amber</td>
<td>LED AMBER 591NM DIFF LENS 2012</td>
<td>Sharp Microelectronics</td>
<td>LT1Z40A</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>D5</td>
<td>2V Zener</td>
<td>DIODE ZENER 2V 500MW SOD123</td>
<td>Diodes Inc</td>
<td>BZT52C2V0-7-F</td>
</tr>
<tr>
<td>12</td>
<td>3</td>
<td>D6, D7, D8</td>
<td>ESD diode</td>
<td>SUPPRESSOR ESD 5VDC 0603 SMD</td>
<td>Bourns Inc.</td>
<td>CG0603MLC-05LE</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>D9</td>
<td>RGB LED</td>
<td>LED RED/BLUE/BLUE PLCC4 SMD</td>
<td>Cree, Inc.</td>
<td>CLV1A-FKB-CJ1M1F1BB7R4S3</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>D10</td>
<td>Status LED Green</td>
<td>LED GREEN CLEAR 0805 SMD</td>
<td>Chicago Miniature</td>
<td>CMD17-21VGC/TR8</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>F1</td>
<td>FUSE</td>
<td>PTC Resetttable Fuses 15Volts 100Amps</td>
<td>Bourns</td>
<td>MF-MSMF050-2</td>
</tr>
<tr>
<td>16</td>
<td>2</td>
<td>J1, J4</td>
<td>8x1 RECP</td>
<td>CONNECT HEADER FEMALE 8POS .1&quot; GOLD</td>
<td>Sullins Connector Solutions</td>
<td>PPC081LFBN-RC</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>J2</td>
<td>9x2 RECP</td>
<td>CONNECT HEADER FMAL 18PS.1&quot; DL GOLD</td>
<td>Sullins Connector Solutions</td>
<td>PPC092LFBN-RC</td>
</tr>
<tr>
<td>18</td>
<td>1</td>
<td>J3</td>
<td>10x1 RECP</td>
<td>CONNECT HEADER FEMALE 10POS .1&quot; GOLD</td>
<td>Sullins Connector Solutions</td>
<td>PPC101LFBN-RC</td>
</tr>
<tr>
<td>19</td>
<td>1</td>
<td>J6</td>
<td>50MIL KEYED SMD</td>
<td>CONNECT HEADER 10 PIN 50MIL KEYED SMD</td>
<td>Samtec</td>
<td>FTSH-105-01-L-DV-K</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>J8</td>
<td>6x2 RECP</td>
<td>CONNECT HEADER FMAL 12PS.1&quot; DL GOLD</td>
<td>Sullins Connector Solutions</td>
<td>PPC062LFBN-RC</td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>J9</td>
<td>3p_jumper</td>
<td>CONNECT HEADER VERT SGL 3POS GOLD</td>
<td>3M</td>
<td>961103-6404-AR</td>
</tr>
<tr>
<td>22</td>
<td>1</td>
<td>J10</td>
<td>USB Mini B</td>
<td>CONNECT USB MINI AB SMT RIGHT ANGLE</td>
<td>TE Connectivity</td>
<td>1734035-2</td>
</tr>
<tr>
<td>No.</td>
<td>Qty</td>
<td>Reference</td>
<td>Value</td>
<td>Description</td>
<td>Manufacturer</td>
<td>Mfr Part Number</td>
</tr>
<tr>
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<td>-------</td>
<td>-------------</td>
<td>--------------</td>
<td>----------------</td>
</tr>
<tr>
<td>23</td>
<td>1</td>
<td>J13</td>
<td>2p_jumper</td>
<td>CONN HEADER VERT SGL 2POS GOLD</td>
<td>3M</td>
<td>961102-6404-AR</td>
</tr>
<tr>
<td>24</td>
<td>3</td>
<td>Q1,Q2,Q3</td>
<td>PMOS</td>
<td>MOSFET P-CH 30V 3.8A SOT23-3</td>
<td>Diodes Inc</td>
<td>DMP3098L-7</td>
</tr>
<tr>
<td>25</td>
<td>1</td>
<td>R3</td>
<td>560 Ω</td>
<td>RES 560 Ω 1/8W 5% 0805 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-6GEYJ561V</td>
</tr>
<tr>
<td>26</td>
<td>12</td>
<td>R4,R11,R12,R14,R15,R16,R24,R25,R32,R33,R34,R45</td>
<td>ZERO</td>
<td>RES 0.0 Ω 1/10W 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3GEY0R00V</td>
</tr>
<tr>
<td>27</td>
<td>1</td>
<td>R5</td>
<td>ZERO</td>
<td>RES 0.0 Ω 1/8W 0805 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-6GEY0R00V</td>
</tr>
<tr>
<td>28</td>
<td>4</td>
<td>R8,R9,R22,R23</td>
<td>2.2K</td>
<td>RES 2.2 kΩ 1/10W 5% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3GEYJ222V</td>
</tr>
<tr>
<td>29</td>
<td>2</td>
<td>R10,R41</td>
<td>4.7K</td>
<td>RES 4.7 kΩ 1/10W 5% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3GEYJ472V</td>
</tr>
<tr>
<td>30</td>
<td>1</td>
<td>R13</td>
<td>100K</td>
<td>RES 100 kΩ 1/10W 5% 0402 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-2GEJ104X</td>
</tr>
<tr>
<td>31</td>
<td>5</td>
<td>R17,R18,R19,R20,R21</td>
<td>560 Ω</td>
<td>RES 560 Ω 1/10W 5% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3GEYJ561V</td>
</tr>
<tr>
<td>32</td>
<td>2</td>
<td>R26, R27</td>
<td>22E</td>
<td>RES 22 Ω 1/10W 1% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3EKF22R0V</td>
</tr>
<tr>
<td>33</td>
<td>1</td>
<td>R28</td>
<td>2.2K</td>
<td>RES 2.2 kΩ 1/8W 5% 0805 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-6GEYJ222V</td>
</tr>
<tr>
<td>34</td>
<td>2</td>
<td>R29,R30</td>
<td>1.5K</td>
<td>RES 1.5 kΩ 1/8W 5% 0805 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-6GEYJ152V</td>
</tr>
<tr>
<td>35</td>
<td>1</td>
<td>R31</td>
<td>330 Ω</td>
<td>RES 330 Ω 1/8W 5% 0805 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-6GEYJ331V</td>
</tr>
<tr>
<td>36</td>
<td>1</td>
<td>R35</td>
<td>232 Ω</td>
<td>RES 232 Ω 1/10W 1% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3EKF2320V</td>
</tr>
<tr>
<td>37</td>
<td>1</td>
<td>R36</td>
<td>120 Ω</td>
<td>RES 120 Ω 1/10W 1% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3EKF1200V</td>
</tr>
<tr>
<td>38</td>
<td>2</td>
<td>R37,R39</td>
<td>1.5K</td>
<td>RES 1.5 kΩ 1/10W 5% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3GEYJ152V</td>
</tr>
<tr>
<td>39</td>
<td>2</td>
<td>R38,R40</td>
<td>3K</td>
<td>RES 3.0 kΩ 1/10W 5% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3GEYJ302V</td>
</tr>
<tr>
<td>40</td>
<td>1</td>
<td>R42</td>
<td>1K</td>
<td>RES 1k Ω 1/8W 5% 0805 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-6GEYJ102V</td>
</tr>
<tr>
<td>41</td>
<td>1</td>
<td>R43</td>
<td>442 Ω</td>
<td>RES 442 Ω 1/10W 1% 0603 SMD</td>
<td>Panasonic - ECG</td>
<td>ERJ-3EKF4420V</td>
</tr>
<tr>
<td>42</td>
<td>2</td>
<td>SW1,SW2</td>
<td>SW PUSH-BUTTON</td>
<td>SWITCH TACTILE SPST-NO 0.05A 12V</td>
<td>Panasonic - ECG</td>
<td>EVQ-PE105K</td>
</tr>
<tr>
<td>43</td>
<td>1</td>
<td>TP5</td>
<td>BLACK</td>
<td>TEST POINT PC MINI .040&quot;D Black</td>
<td>Keystone Electronics</td>
<td>5001</td>
</tr>
<tr>
<td>44</td>
<td>2</td>
<td>TVS1,TVS2</td>
<td>5V 350W</td>
<td>TVs UNIDIR 350W 5V SOD-323</td>
<td>Dioded Inc.</td>
<td>SD05-7</td>
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<td>TVS4</td>
<td>18V 350W</td>
<td>TVs DIODE 18V 1CH BI SMD</td>
<td>Bourns Inc.</td>
<td>CDSOD323-T18C</td>
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<td>46</td>
<td>1</td>
<td>U1</td>
<td>NCP1117DTARKG</td>
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<td>47</td>
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<td>U2</td>
<td>PSoC 4 (CY8C4245AXI-483)</td>
<td>44TQFP PSoC4A target chip</td>
<td>Cypress Semiconductor</td>
<td>CY8C4245AXI-483</td>
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<td>48</td>
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<td>U3</td>
<td>PSoC 5LP (CY8CS868LTI-LP039)</td>
<td>68QFN PSoC 5LP chip for USB debug channel and USB-Serial interface</td>
<td>Cypress Semiconductor</td>
<td>CY8CS868LTI-LP039</td>
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No Load Components

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<tr>
<th>No.</th>
<th>Qty</th>
<th>Reference</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Mfr Part Number</th>
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<tr>
<td>49</td>
<td>1</td>
<td>C29</td>
<td>1.0 uFd</td>
<td>CAP CERAMIC 1.0UF 25V X5R 0603 10%</td>
<td>Taiyo Yuden</td>
<td>TMK107BJ105KA-T</td>
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### Regulatory Compliance Information

The CY8CKIT-042 PSoC 4 Pioneer Kit has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations:

- EN 55022:2010 Class A - Emissions
- EN 55024:2010 Class A - Immunity

### Parts List

<table>
<thead>
<tr>
<th>No.</th>
<th>Qty</th>
<th>Reference</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Mfr Part Number</th>
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<tr>
<td>50</td>
<td>1</td>
<td>J5</td>
<td>6X1 RECP RA</td>
<td>CONN FEMALE 6POS .100&quot; R/A GOLD</td>
<td>Sullins Connector Solutions</td>
<td>PPC061LGBN-RC</td>
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<tr>
<td>51</td>
<td>1</td>
<td>J7</td>
<td>50MIL KEYED SMD</td>
<td>CONN HEADER 10 PIN 50MIL KEYED SMD</td>
<td>Samtec</td>
<td>FTXH-105-01-L-DV-K</td>
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<td>J11</td>
<td>2 PIN HDR</td>
<td>CONN HEADER FEMALE 2POS .1&quot; GOLD</td>
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<td>J12</td>
<td>3x2 RECPT</td>
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<td>5</td>
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<td>RES 0.0 Ω 1/10W 0603 SMD</td>
<td>Panasonic-ECG</td>
<td>ERJ-3GEY0R00V</td>
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<td>R6</td>
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<td>TEST POINT PC MINI .040&quot;D RED</td>
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<td>5000</td>
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<td>TVS UNIDIR 350W 5V SOD-323</td>
<td>Diode Inc.</td>
<td>SD05-7</td>
</tr>
</tbody>
</table>

**Special Jumper Installation Instructions**

- **Install jumper across pins 1 and 2**
  - Rectangular Connectors MINI JUMPER GF 6.0MM CLOSE TYPE BLACK
  - Kobiconn | 151-8010-E
  - Kobiconn | 151-8010-E

**Label**

- **LBL, Kit Product Identification Label, Vendor Code, Datecode, Serial Number CY8CKIT-042 Rev** (YYWWW-VXXXXX)
  - Cypress Semiconductor
- **LBL, PCBA Anti-Static Warning, 10mm X 10mm**
  - Cypress Semiconductor
- **Assembly Adhesive Label, Manufacturing ID**
  - Cypress Semiconductor
- **Kit QR code**
  - Cypress Semiconductor