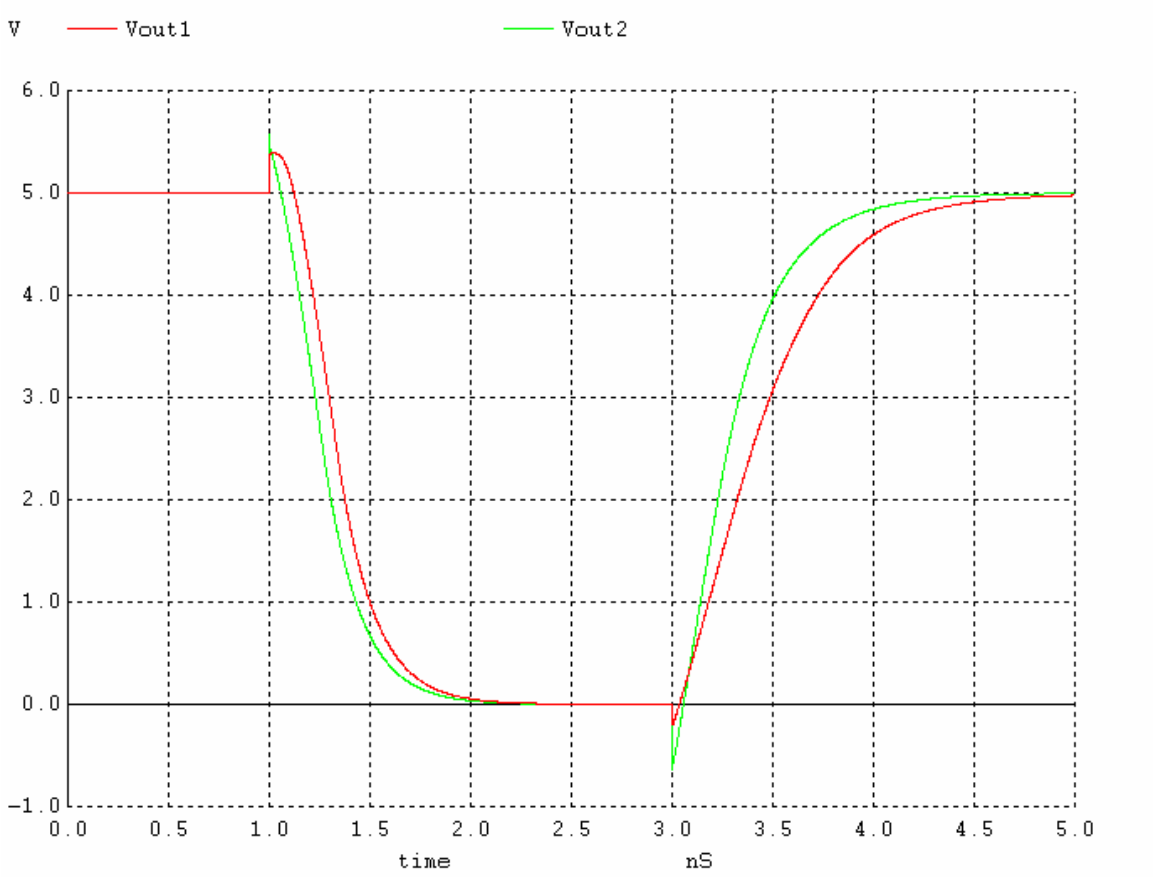
Speed of NAND

Effect of which input varies

```
*CMOS 2-Input NAND

*Control section determines type of analysis
.control
destroy all
echo
TRAN 0.001nS 5nS
plot Vout0 Vout1  Vout2
.endc


VVdd Vdd 0 DC 5


**********************************************************************
*****
*Both inputs change
*form of pulse -- PULSE(V1 V2 TD TR TF PW PER)
VVa0 Va0 0 PULSE(0 5 1ns 0 0 2ns 4ns)
VVb0 Vb0 0 PULSE(0 5 1ns 0 0 2ns 4ns)

M01 Vout0 Va0 Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M02 Vout0 Vb0 Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M03 1 Va0 0 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u
M04 Vout0 Vb0 1 0 MNMOSIS L=2u W=6u AD=36p PD=24u AS=12p PS=16u

**********************************************************************
*****
*Input A (lower input) changes
*form of pulse -- PULSE(V1 V2 TD TR TF PW PER)
VVa1 Va1 0 PULSE(0 5 1ns 0 0 2ns 4ns)
VVb1 Vb1 0 DC 5V

M11 Vout1 Va1 Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M12 Vout1 Vb1 Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M13 11 Va1 0 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u
M14 Vout1 Vb1 11 0 MNMOSIS L=2u W=6u AD=36p PD=24u AS=12p PS=16u

**********************************************************************
******
*Input B (upper input) changes
*form of pulse -- PULSE(V1 V2 TD TR TF PW PER)
VVa2 Va2 0 DC 5V
VVb2 Vb2 0 PULSE(0 5 1ns 0 0 2ns 4ns)

M21 Vout2 Va2 Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M22 Vout2 Vb2 Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M23 21 Va2 0 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u
M24 Vout2 Vb2 21 0 MNMOSIS L=2u W=6u AD=36p PD=24u AS=12p PS=16u


.MODEL MNMOSIS NMOS LEVEL=2 LD=0.250000U TOX=418.000008E-10
+ NSUB=9.236187E+14 VTO=0.858153 KP=5.048000E-05 GAMMA=0.198
+ PHI=0.6 UO=596.729 UEXP=7.029586E-02 UCRIT=10266.7
+ DELTA=2.7371 VMAX=65701.4 XJ=0.250000U LAMBDA=1.843384E-02
+ NFS=1.086360E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.760000 CGDO=3.097916E-10 CGSO=3.097916E-10 CGBO=3.838441E-10
+ CJ=8.997900E-05 MJ=0.783638 CJSW=5.524800E-10 MJSW=0.285064
PB=0.800000

.MODEL MPMOSIS PMOS LEVEL=2 LD=0.250000U TOX=418.000008E-10
+ NSUB=9.309300E+15 VTO=-0.889271 KP=1.908000E-05 GAMMA=0.6289
+ PHI=0.6 UO=216.28 UEXP=0.218144 UCRIT=62664
+ DELTA=0.164572 VMAX=100000 XJ=0.250000U LAMBDA=5.011626E-02
+ NFS=9.266623E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=66.820000 CGDO=3.097916E-10 CGSO=3.097916E-10 CGBO=3.727276E-10
+ CJ=2.981300E-04 MJ=0.556944 CJSW=3.002100E-10 MJSW=0.243045
PB=0.800000

.END
```

Effect of which input varies

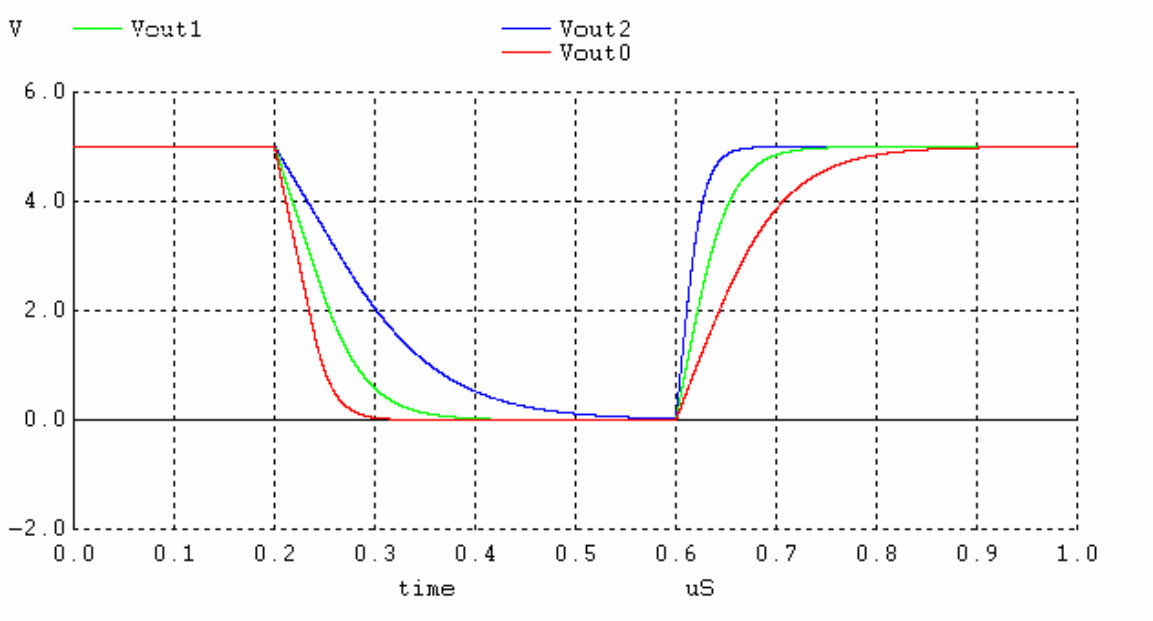


Red –	Only A (lower) changes	$t_{p,HL}$=0.30nS	$t_{p,LH}$=0.42nS
Green –	Only B (upper) changes	$t_{p,HL}$=0.27nS	$t_{p,LH}$=0.28nS

*CMOS NAND Size comparison

```
*Control section determines type of analysis
.control
destroy all
echo
TRAN 0.001nS 5nS
plot Vout0 Vout1  Vout2
.endc


VVdd Vdd 0 DC 5
*form of pulse -- PULSE(V1 V2 TD TR TF PW PER)
VVin Vin 0 PULSE(0 5 1ns 0 0 2ns 4ns)

**********************************************************************
*****
*Invertor

M01 Vout0 Vin Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M02 Vout0 Vin 0 0 MNMOSIS L=2u W=6u AD=36p PD=24u AS=12p PS=16u

**********************************************************************
*****
*2 input NAND
M11 Vout1 Vin Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M12 Vout1 Vin Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M13 11 Vin 0 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u
M14 Vout1 Vin 11 0 MNMOSIS L=2u W=6u AD=36p PD=24u AS=12p PS=16u

**********************************************************************
******
*4 input NAND
M21 Vout2 Vin Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M22 Vout2 Vin Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M23 Vout2 Vin Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M24 Vout2 Vin Vdd Vdd MPMOSIS L=2u W=6u AD=48p PD=28u AS=72p PS=48u
M25 Vout2 Vin 21 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u
M26 21 Vin 22 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u
M27 22 Vin 23 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u
M28 23 Vin 0 0 MNMOSIS L=2u W=6u AD=12p PD=16u AS=36p PS=24u


.MODEL MNMOSIS NMOS LEVEL=2 LD=0.250000U TOX=418.000008E-10
+ NSUB=9.236187E+14 VTO=0.858153 KP=5.048000E-05 GAMMA=0.198
+ PHI=0.6 UO=596.729 UEXP=7.029586E-02 UCRIT=10266.7
+ DELTA=2.7371 VMAX=65701.4 XJ=0.250000U LAMBDA=1.843384E-02
+ NFS=1.086360E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.760000 CGDO=3.097916E-10 CGSO=3.097916E-10 CGBO=3.838441E-10
+ CJ=8.997900E-05 MJ=0.783638 CJSW=5.524800E-10 MJSW=0.285064
PB=0.800000

.MODEL MPMOSIS PMOS LEVEL=2 LD=0.250000U TOX=418.000008E-10
+ NSUB=9.309300E+15 VTO=-0.889271 KP=1.908000E-05 GAMMA=0.6289
+ PHI=0.6 UO=216.28 UEXP=0.218144 UCRIT=62664
+ DELTA=0.164572 VMAX=100000 XJ=0.250000U LAMBDA=5.011626E-02
+ NFS=9.266623E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=66.820000 CGDO=3.097916E-10 CGSO=3.097916E-10 CGBO=3.727276E-10
+ CJ=2.981300E-04 MJ=0.556944 CJSW=3.002100E-10 MJSW=0.243045
PB=0.800000

.END
```

Add 10 pF load capacitor between Vout and ground



$t_{p,HL}$ are 28, 45 and 0.94 nS for invertor, 2 input, 4 input.
$t_{p,LH}$ are all about 56, 28, and 14 nS for invertor, 2 input, 4 input.

$t_{p,HL}$ speed goes approximately as N, $t_{p,LH}$ goes roughly as 1/N

$$t_{p,HL} = \frac{C_{load}}{k_n' \frac{W_n}{L_n}\left(V_{dd} - V_{T,n}\right)} \left[\frac{2V_{T,n}}{V_{dd} - V_{T,n}} + \ln\left(\frac{4\left(V_{dd} - V_{T,n}\right)}{V_{dd}} - 1 \right) \right]$$

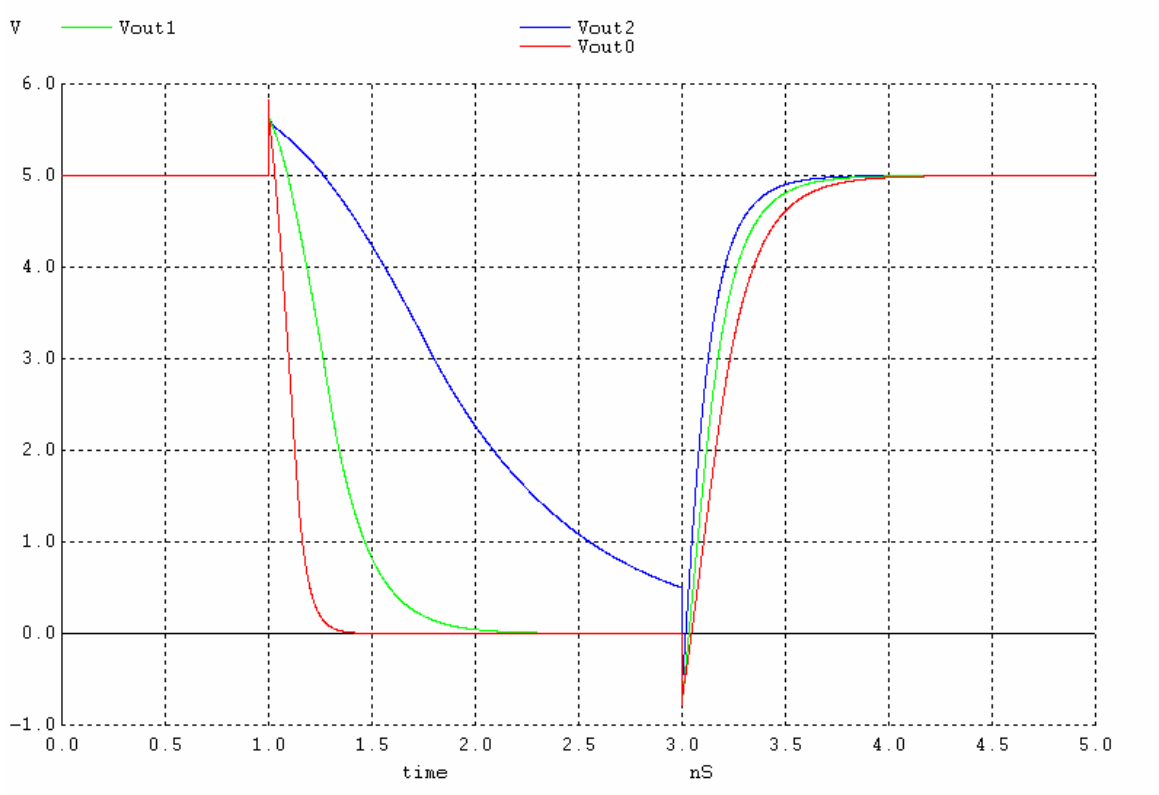
For invertor, W_n/L_n=6/2=3. $t_{p,HL}$=20nS
For 2 input nand, W_n/L_n=6/4=1.5. $t_{p,HL}$=40nS
For 4 input nand, W_n/L_n=6/8=0.75. $t_{p,HL}$=80nS

$$t_{p,LH} = \frac{C_{load}}{k_p' \frac{W_p}{L_p}\left(V_{dd} - \left|V_{T,p}\right|\right)} \left[\frac{2\left|V_{T,p}\right|}{V_{dd} - \left|V_{T,p}\right|} + \ln\left(\frac{4\left(V_{dd} - \left|V_{T,p}\right|\right)}{V_{dd}} - 1 \right) \right]$$

For invertor, W_p/L_p=6/2=3. t_{pLH}=54nS
For 2 input nand, W_p/L_p=12/2=6. $t_{p,HL}$=27nS
For 4 input nand, W_p/L_p=24/2=12. $t_{p,HL}$=13nS

No external load capacitor (only parasitics)

Note different time scale.



$t_{p,HL}$ are 0.11, 0.30 and 0.94 nS for invertor, 2 input, 4 input.
$t_{p,LH}$ are all about 0.19, 0.14, and 0.10 nS for invertor, 2 input, 4 input.

$t_{p,HL}$ speed goes approximately as $(N+N^2)$, $t_{p,LH}$ is roughly constant (resistance decreases, but capacitance increases)

if N=1, $(N+N^2)=2$
if N=2, $(N+N^2)=5$
if N=4, $(N+N^2)=20$