Problem 1) Using our MOS transistor models, CMOS has 0 static power dissipation. Briefly (one or two sentences) explain why,

\[
V_{	ext{in}} \text{ MOS are in series. NMOS is off when } V_i = 0 \Rightarrow i_D = 0 \\
PMOS is off when } V_i = 5 \Rightarrow i_D = 0
\]

Problem 2) Using our MOS transistor models, CMOS has \( V_{OL} = 0, V_{OH} = V_{DD} \). Briefly (one or two sentences) explain why,

\[
V_i = 0, \text{ NMOS OFF, PMOS ON, } i_D = 0, \text{ } U_{S,D} = 0, \text{ } U_D = V_{DD} \\
V_i = V_{OL}, \text{ NMOS OFF, PMOS ON, } i_D = 0, \text{ } U_{S,D} = 0, \text{ } U_D = V_{DD} = 0
\]

Problem 3) We have only briefly mentioned subthreshold conduction in which current can flow in a transistor even when there is no induced channel (for NMOS, \( V_{GS} < V_T \)). The subthreshold conduction can be modeled as:

\[
i_D = I_{d,ST} e^{\frac{V_{GS} - V_T}{0.025}} \left( 1 - e^{-\frac{V_{DS}}{0.025}} \right)
\]

Set up the equations to show how you would use Newton’s Method to find the drain current. Note that \( V_{in} = 0V \).

\[
i_0 = \frac{I_{d,ST} e^{\frac{V_G}{0.025}} \left( 1 - e^{-\frac{V_{DS}}{0.025}} \right)}{I_0} = \frac{V_{GS} - V_D}{R} \\
\text{Proc same equation as a} \ \text{reverse biased diode, which acts as current source.}
\]

\[
f^' (V_0) = \frac{I_0}{0.025} e^{-\frac{V_D}{0.025}} + \frac{1}{R}
\]

\[
V_{max} = V_{current} = \int \left( V_0 \right) - \frac{V_{max}}{R}
\]

\[
f^' (V_0) = \frac{I_0}{I_0} e^{-\frac{V_D}{0.025}} + \frac{1}{R}
\]
Problem 4) Using $V_T = 1V$, $I_{d,s} = 1E^{-15}A$ iterate until successive changes in $V_{DS}$ are less than 0.05 volts, or for 3 iterations, whichever comes first. Fill in the table starting with an initial guess of 4.7V. This may take some time – you may want to complete the exam and come back to this – I have blank paper if you need it. Be neat.

What is $i_D$?

<table>
<thead>
<tr>
<th>Iteration</th>
<th>Initial Guess</th>
<th>1\textsuperscript{st} iteration</th>
<th>2\textsuperscript{nd} iteration</th>
<th>3\textsuperscript{rd} iteration</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>2.5</td>
<td>5</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

$v_D = 2.5 \quad f(v_D) = -7.5 \times 10^{-5} \quad f'(v_D) = 1 \times 10^{-5}$

$v_D = 5 \quad f(v_D) = 4.7 \times 10^{-33} \quad 1 \times 10^{-5}$

$v_{GS}$

$i_D = 4.7 \times 10^{-38}A$
Problem 5) Did your solution to the previous problem converge quickly? Why or why not?

Convexes in linear region act as reverse biased diode (i.e., a current source), so it looks like linear circuit.

Problem 6) How would you change your analysis to estimate the current in a CMOS inverter when $V_{in}=0V$? Could you come up with a good estimate without needing more complicated equations than those used previously? Be specific, but don’t actually do any calculations.

Use linear region approximation for PMOS $I_{D} \approx \frac{k_{P}w}{2L} (V_{GS} - V_{T}) V_{DD}$

$$I_{D} \approx \frac{k_{P}w}{2L} V_{DD} \frac{2L}{k_{P}w(V_{GS} - V_{T})}$$

Also assume $R_{D}$ has little effect on final answer. In reverse biased diode with approx. 5V across it, so answer doesn’t change.

There are some situations in which logic families other than CMOS will be useful. One of these families is called “pseudo-NMOS” in which a PMOS transistor with the gate grounded is used as the load for an NMOS transistor. The characteristics of the two transistor are given on the following pages; the range of the axes is identical for all graphs.

Problem 7) For the pseudo-NMOS inverter shown, sketch the input/output characteristics as $V_{in}$ goes from 0 to 5V ($V_{DD}=5V$) – try to be reasonably accurate.

Two sets of axes, estimate $V_{o}$.

![Graph](image-url)
I-V characteristics of an NMOS transistor (second copy, in case you make mistakes drawing on first one).
I-V characteristics of a PMOS transistor (same size as NMOS transistor)

I-V characteristics of a PMOS transistor, with the horizontal axis showing $V_{out}$. 
Problem 8) Calculate $V_{OL}$ (i.e., the output when $V_{in} = V_{DD} = 5V$). Compare with your sketch.

\[
\frac{k_n}{2} \frac{W}{L} \left((V_{GS} - V_{TH})V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{k_n}{2} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2
\]

\[
\frac{k_n}{2} \frac{W}{L} \frac{V_{OL}^2}{2} = 3
\]

\[
3\left((V_{OL} - \frac{V_{OL}^2}{2}) = \left(\frac{V_{DD} - 0}{2}\right)^2
\]

\[
3\left(4V_{OL} - \frac{V_{OL}^2}{2}\right) = 8
\]

\[
\frac{3}{2}V_{OL}^2 - 12V_{OL} + 8 = 0
\]

\[
V_{OL} = \frac{-(-12) \pm \sqrt{(-12)^2 - 4 \times 3 \times 8}}{2 \times 3} = \frac{12 - 9.79}{6} = 0.173
\]

From sketch, $V_{OL}$.

Problem 9) How would you change the size of the PMOS transistor to lower $V_{OL}$?

INCREASE $L$

(DECREASE $W/L$)
**Problem 10)** Each transistor has three specific regions of operation, OFF, LIN, and SAT (LIN=ohmic).

i. Cross out entries of the table that are not applicable to this problem.

ii. Renumber the remaining entries starting with “1” \( V_{in}=0 \) and increasing the numbers as \( V_{in} \) increases to \( V_{DD} \). Very briefly explain

<table>
<thead>
<tr>
<th>N1</th>
<th>P1</th>
<th>#</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>PMOS NEVER ON</td>
</tr>
<tr>
<td>LIN</td>
<td>OFF</td>
<td></td>
</tr>
<tr>
<td>SAT</td>
<td>OFF</td>
<td></td>
</tr>
<tr>
<td>OFF</td>
<td>LIN</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>when ( V_{in} ) is OFF, PMOS LIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 0 \leq V_{in} &lt; 2.5 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{in} = 0 \text{ to } 2.5 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{in} = 3.3 \text{ to } 4.0 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{in} = 1 \text{ to } 3.3 )</td>
</tr>
<tr>
<td>LIN</td>
<td>LIN</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 2.5 \leq V_{in} &lt; 5 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{in} &gt; 4.0 )</td>
</tr>
<tr>
<td>SAT</td>
<td>LIN</td>
<td></td>
</tr>
<tr>
<td>LIN</td>
<td>SAT</td>
<td>4</td>
</tr>
<tr>
<td>SAT</td>
<td>SAT</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Never both SAT</td>
</tr>
</tbody>
</table>

**Problem 11)** For each of the regions listed above, neatly label and set up the equations you would need to solve for \( V_{out} \) vs. \( V_{in} \) throughout the region. Don’t actually solve the equations.

Roughly within a few hundred millivolts, the range of input output voltages for each region from previous prob.
Problem 12) Fill in the truth table for the gate shown. What is it? Note: logic 1 is near Vdd, logic 0 is near 0V. Very briefly explain your reasoning.

\[
\begin{array}{ccc}
&A&=\begin{array}{c}
0\n1
\end{array}
&B&=\begin{array}{c}
0\n1
\end{array}
&C=\begin{array}{c}
0\n1
\end{array}
\end{array}
\]

\[
\begin{array}{c}
\text{A} & B & C \\
\hline
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 1 \\
\end{array}
\]

\[
\begin{array}{c}
M_1 & N_2 \\
\hline
\text{OFF} & \text{OFF} \\
\text{ON} & \text{OFF} \\
\text{OFF} & \text{ON} \\
\text{ON} & \text{ON} \quad \text{BUT OUTPUTS}
\end{array}
\]

XNOR

\[
\begin{array}{c}
&\begin{array}{c}
7
7
7
\end{array} \\
\times & \begin{array}{c}
5
5
5
\end{array} \\
\hline
\begin{array}{c}
35
35
35
\end{array}
\end{array}
\]

"It may be wrong, but it's how I feel."